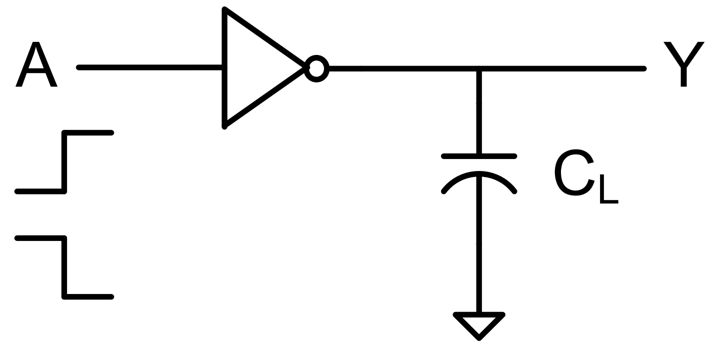
EE 330
Lecture 8

Technology Files

- Design Rules
- Process Flow
- Model Parameters

Response time of logic gates



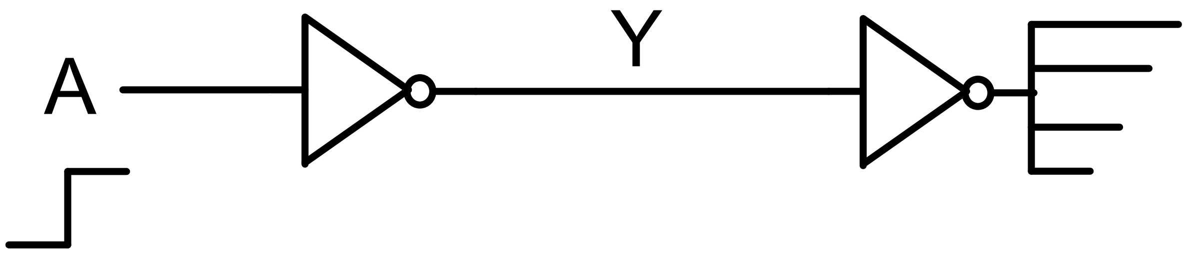
$$t_{HL} \cong R_{SWn} C_L$$

$$t_{LH} \cong R_{SWp} C_L$$

- Logic Circuits can operate very fast
- Extremely small parasitic capacitances play key role in speed of a circuit

Review from Last Time

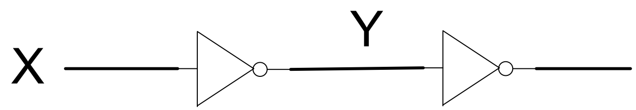
One gate often drives one or more other gates !



What are t_{HL} and t_{LH}?

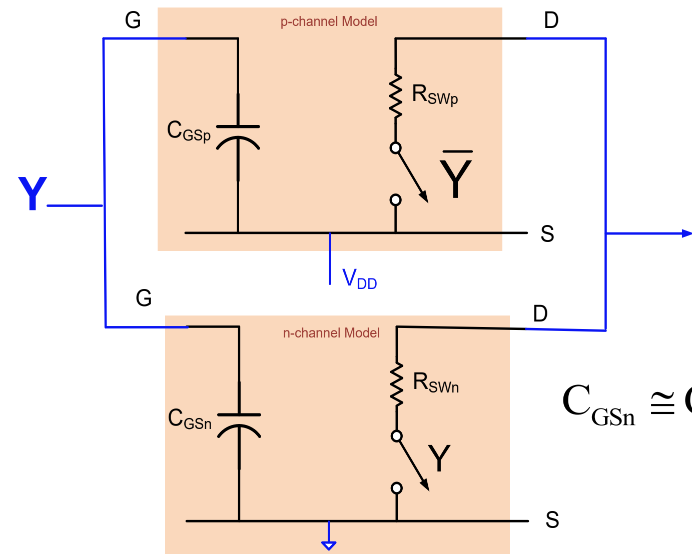
Review from Last Time

Example: What is the delay of a minimum-sized inverter driving another identical device?



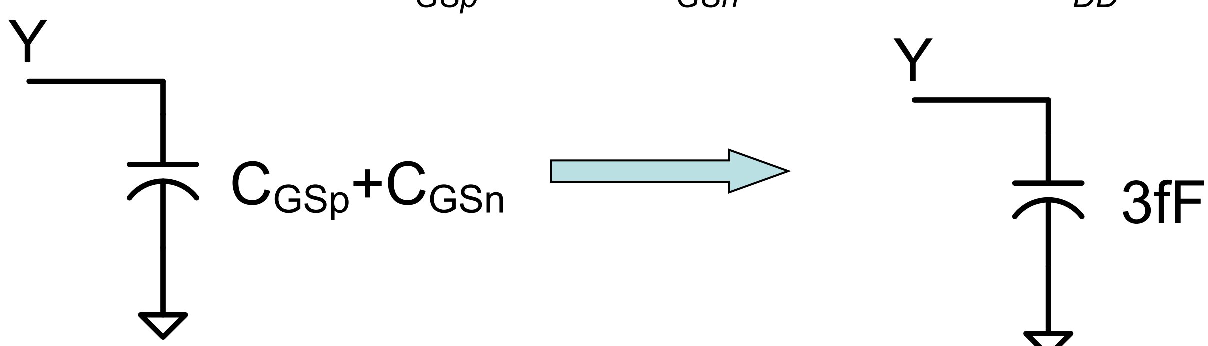
Load on first inverter

C_{GSn} and C_{GSp} both 1.5fF



$$C_{GSn} \cong C_{GSp} \cong 1.5\text{fF}$$

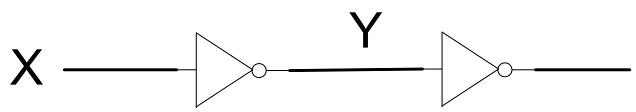
Loading effects same whether C_{GSp} and/or C_{GSn} connected to V_{DD} or GND

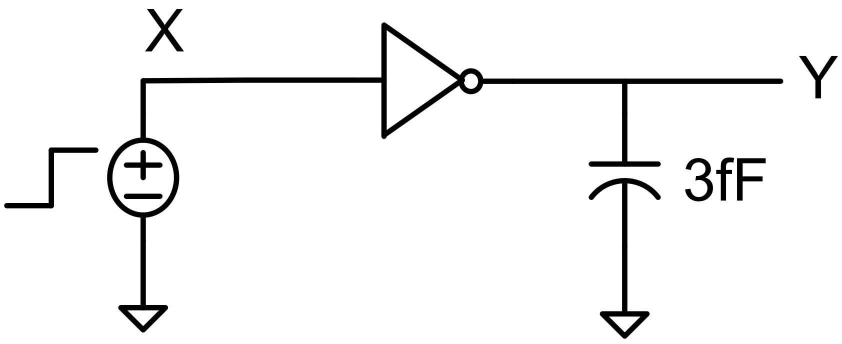


For convenience, will reference both to ground

Review from Last Time

Example: What is the delay of a minimum-sized inverter driving another identical device?





$$t_{HL} \cong R_{SWn} C_L = 2K \bullet 3fF = 6p\,\text{sec}$$

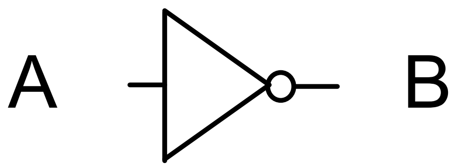
$$t_{LH} \cong R_{SWp} C_L = 6K \bullet 3fF = 18p\,\text{sec}$$

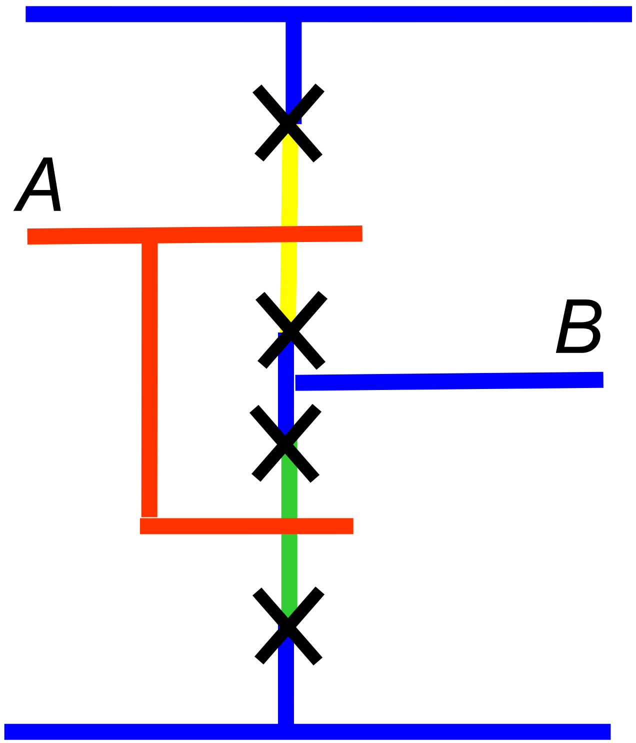
Do gates really operate this fast?

What would be the maximum clock rate for acceptable operation?

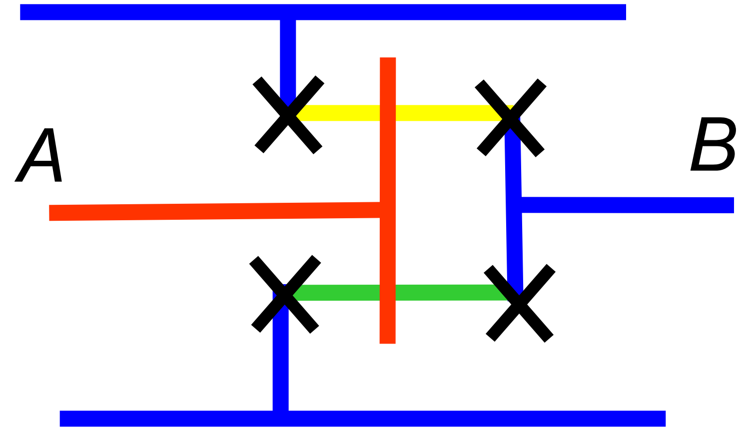
Review from Last Time

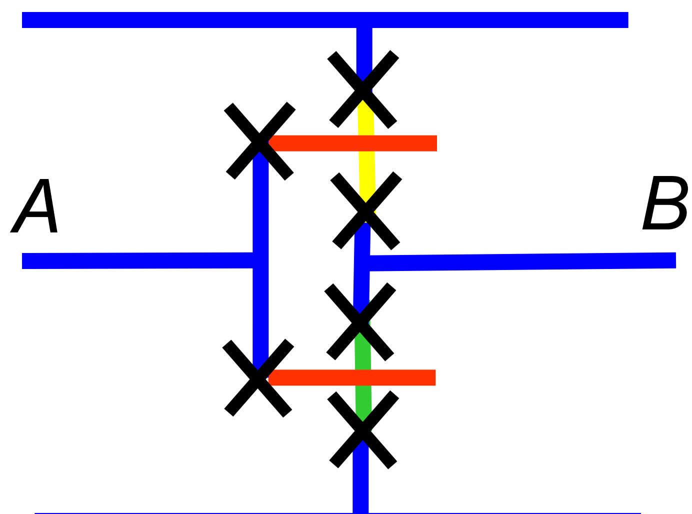
Stick Diagram





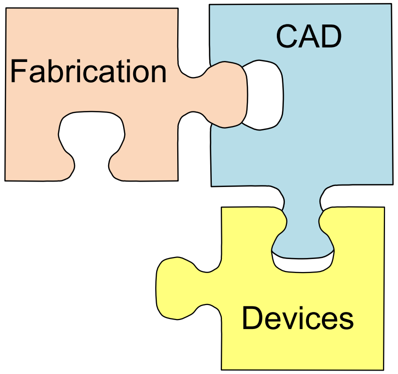
Alternate Representations





Review from Last Time

Technology Files



- Provide Information About Process
  - Design Rules
  - Process Flow (Fabrication Technology)
  - Model Parameters
- Serve as Interface Between Design Engineer and Process Engineer
- Insist on getting information that is deemed important for a design
  - Limited information available in academia
  - Foundries often sensitive to who gets access to information
  - Customer success and satisfaction is critical to foundries

Review from Last Time

Technology Files

- Design Rules
- Process Flow (Fabrication Technology) (will discuss next)
- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

First – A preview of what the technology files look like !

Technology Files

- Design Rules

- Process Flow (Fabrication Technology) (will discuss next)

- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

Design Rules

- Give minimum feature sizes, spacing, and other constraints that are acceptable in a process

- Very large number of devices can be reliably made with the design rules of a process

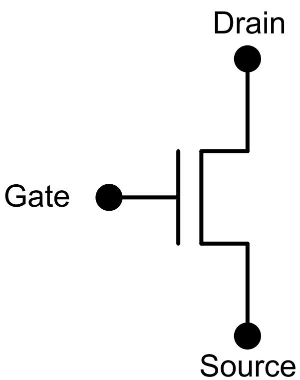
- Yield and performance unpredictable and often low if rules are violated

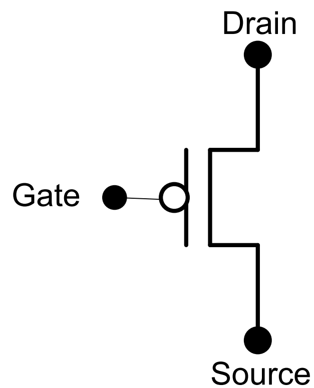
- Compatible with design rule checker in integrated toolsets

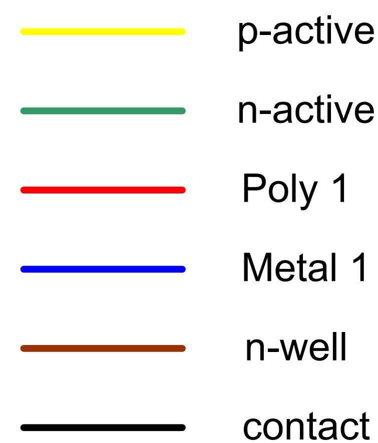
Design Rules and Layout – consider transistors

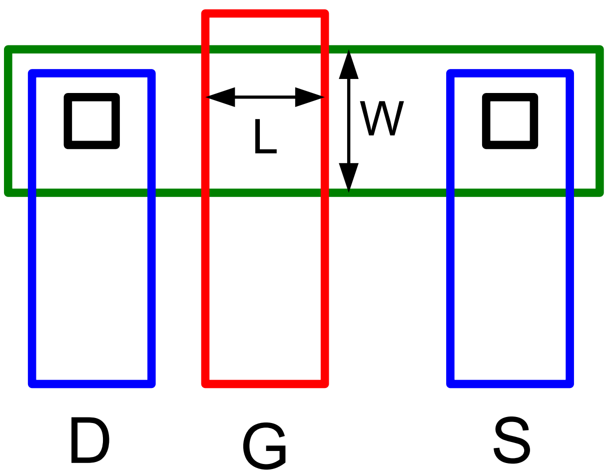
Layer Map

n-well bulk CMOS Process

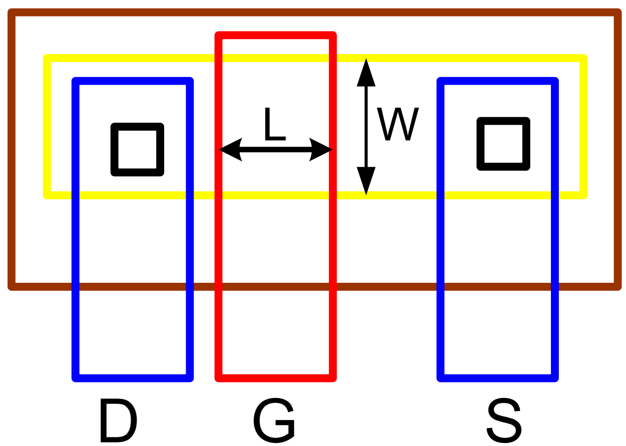








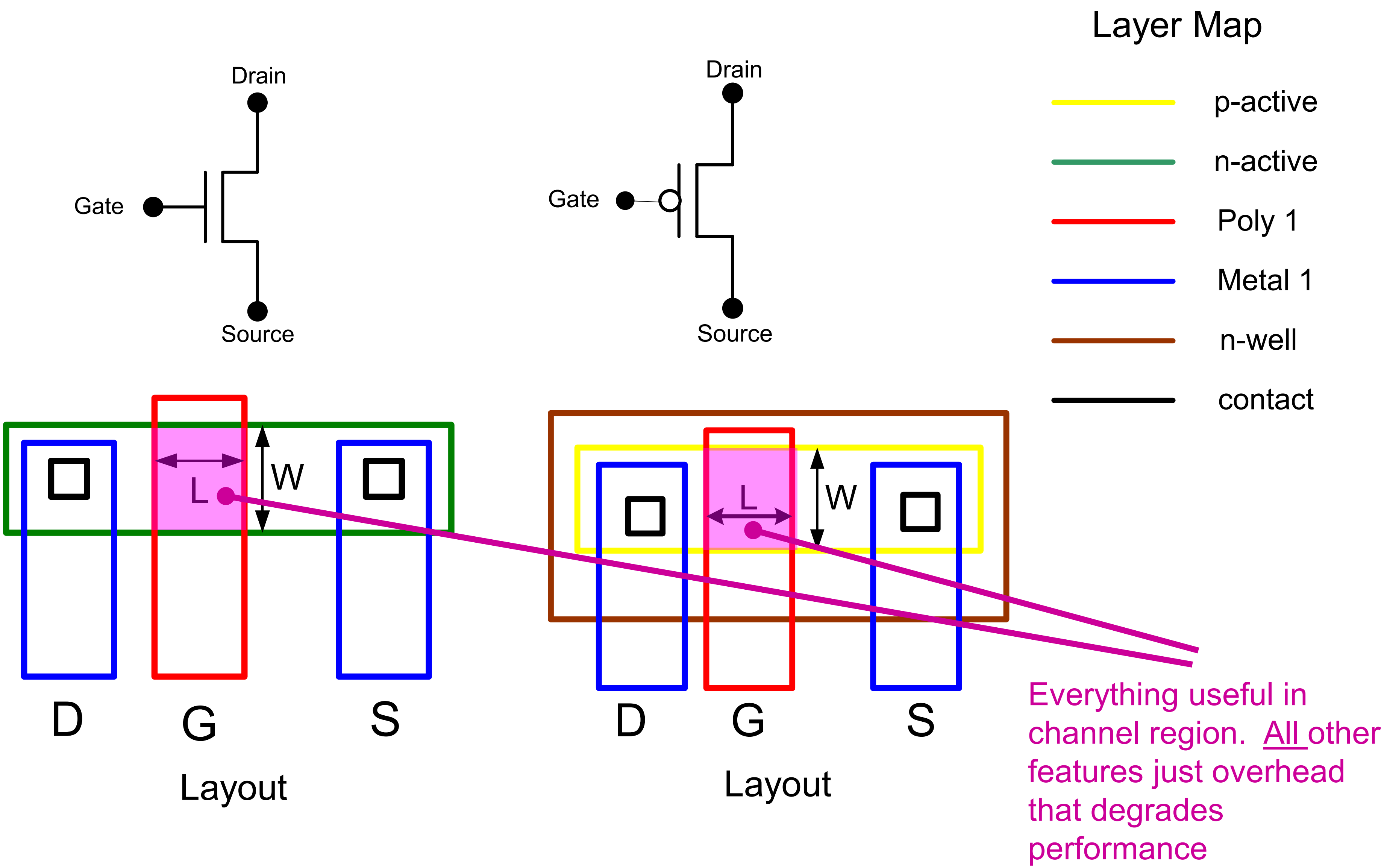
Layout



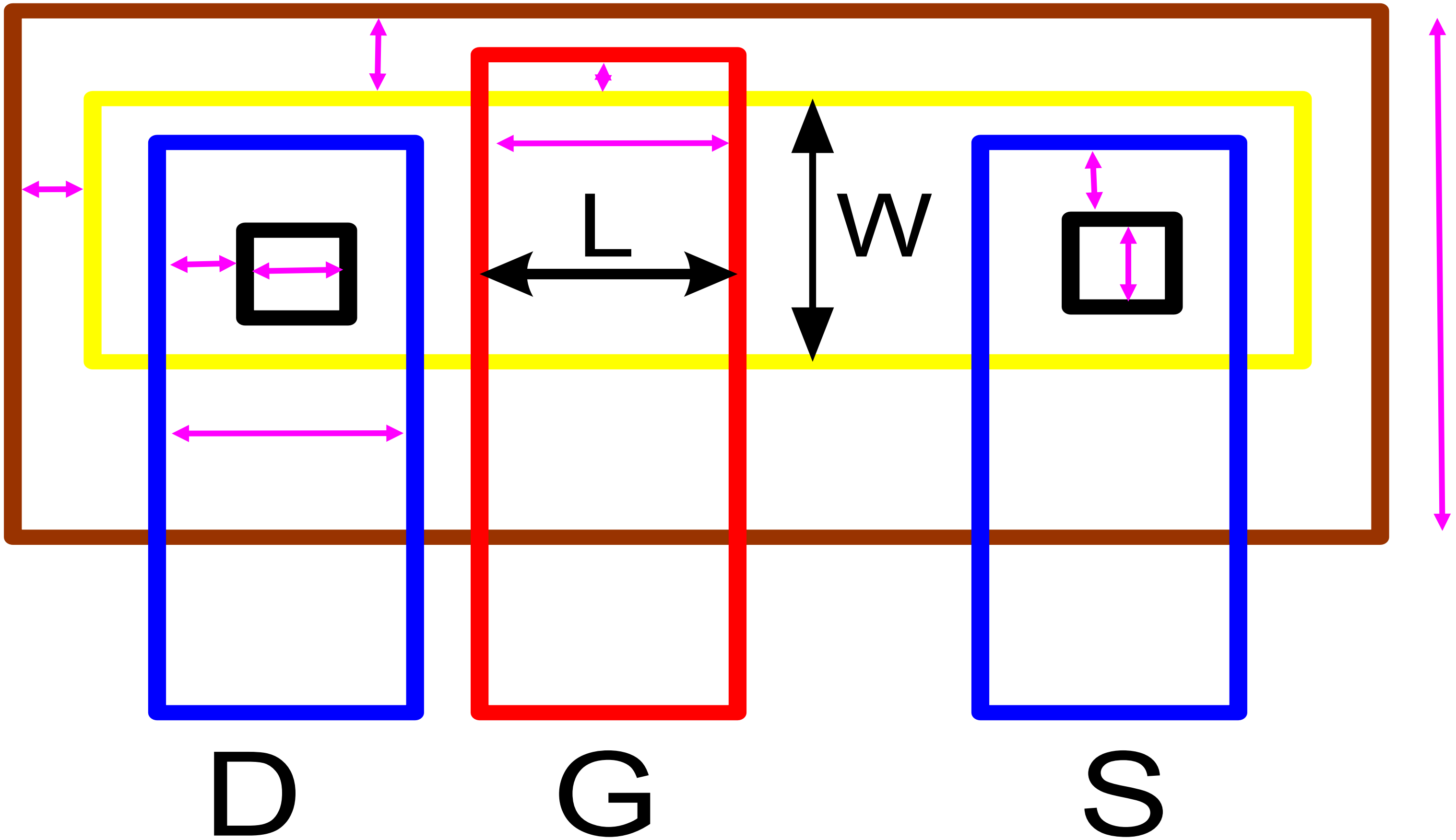
Layout

Layout always represented in a top view in two dimensions

Design Rules and Layout – consider transistors



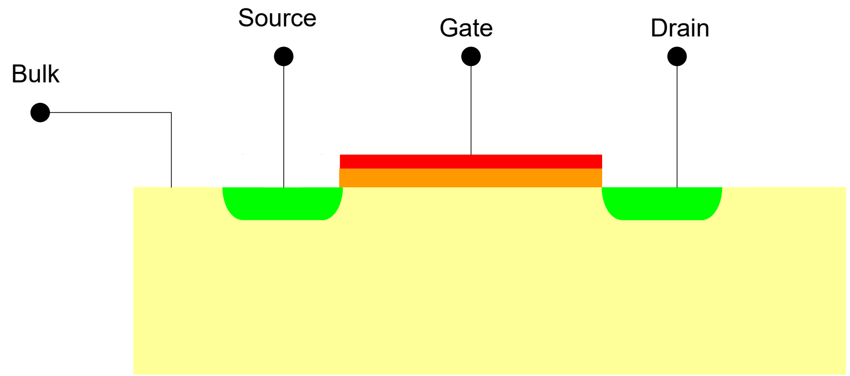
Design Rules



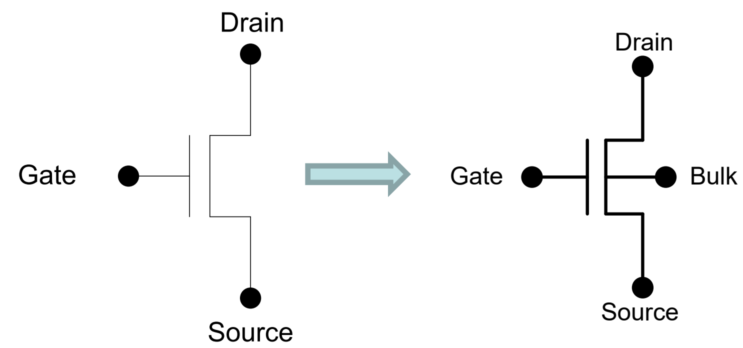
Design rules give minimum feature sizes and spacings

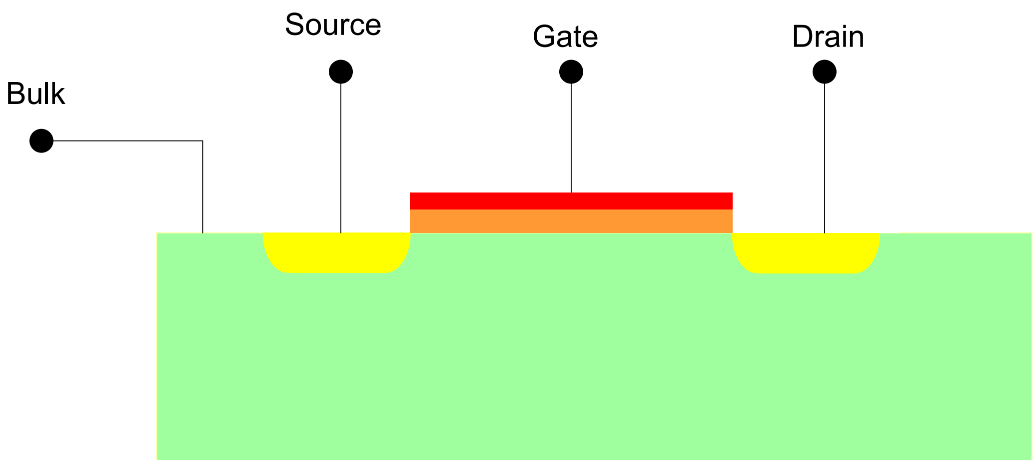
Designers generally do layouts to minimize size of circuit subject to design rule constraints (because yield, cost, and performance usually improve)

MOS Transistor

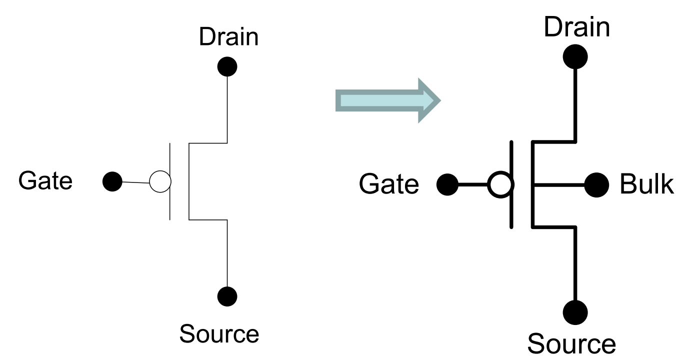


n-channel MOSFET

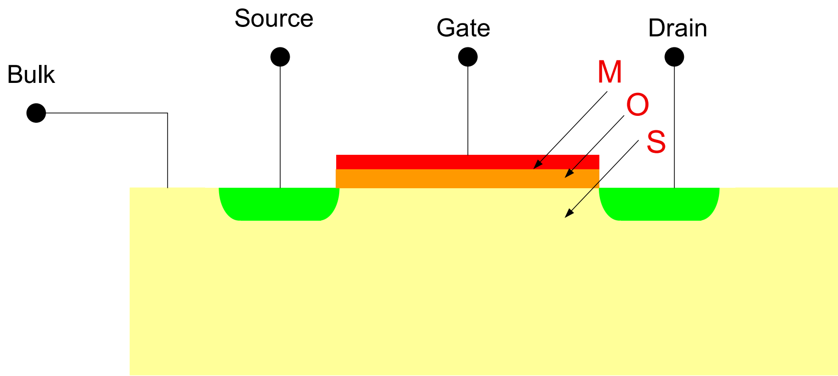




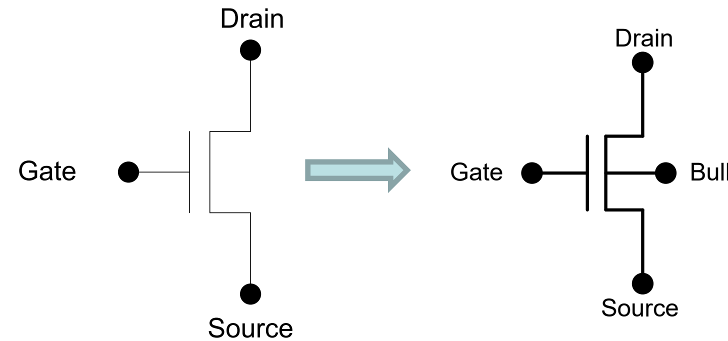
p-channel MOSFET



MOS Transistor Nomenclature



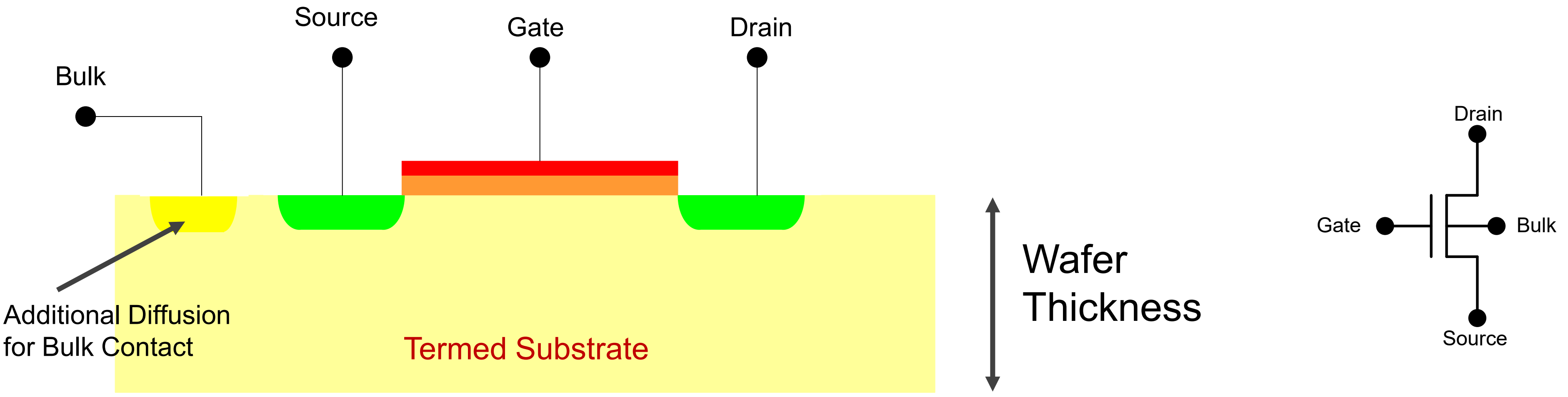
n-channel MOSFET



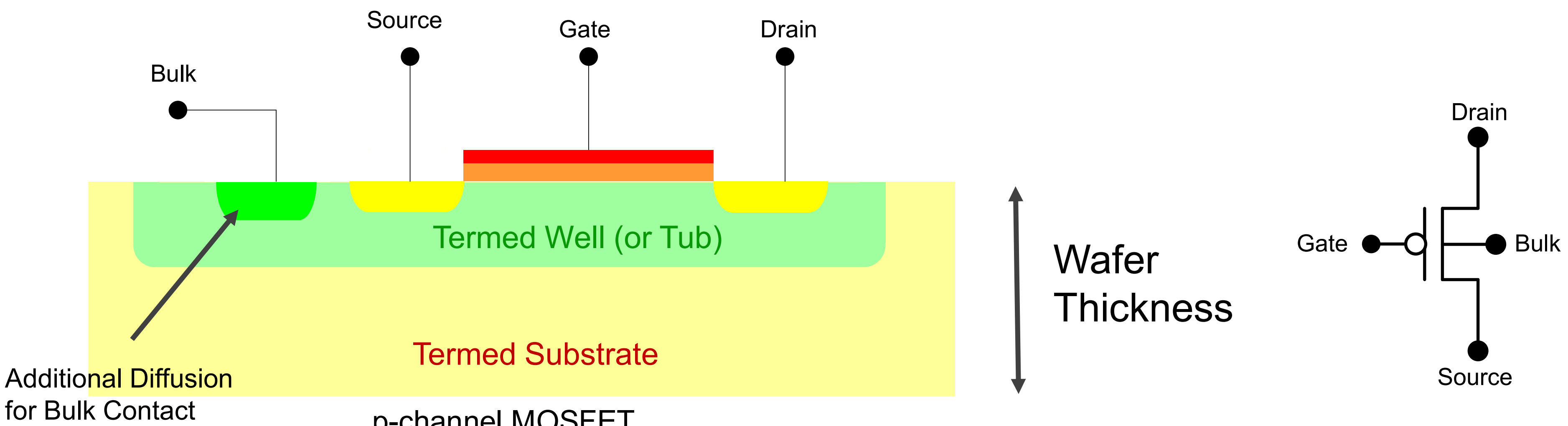
<u>M</u>etal <u>O</u>xide <u>S</u>emiconductor → MOS

Early processes used metal for the gate, today metal is seldom used but the term MOS transistor is standard even though the gate is no longer metal

MOS Transistor in Bulk n-well CMOS Process

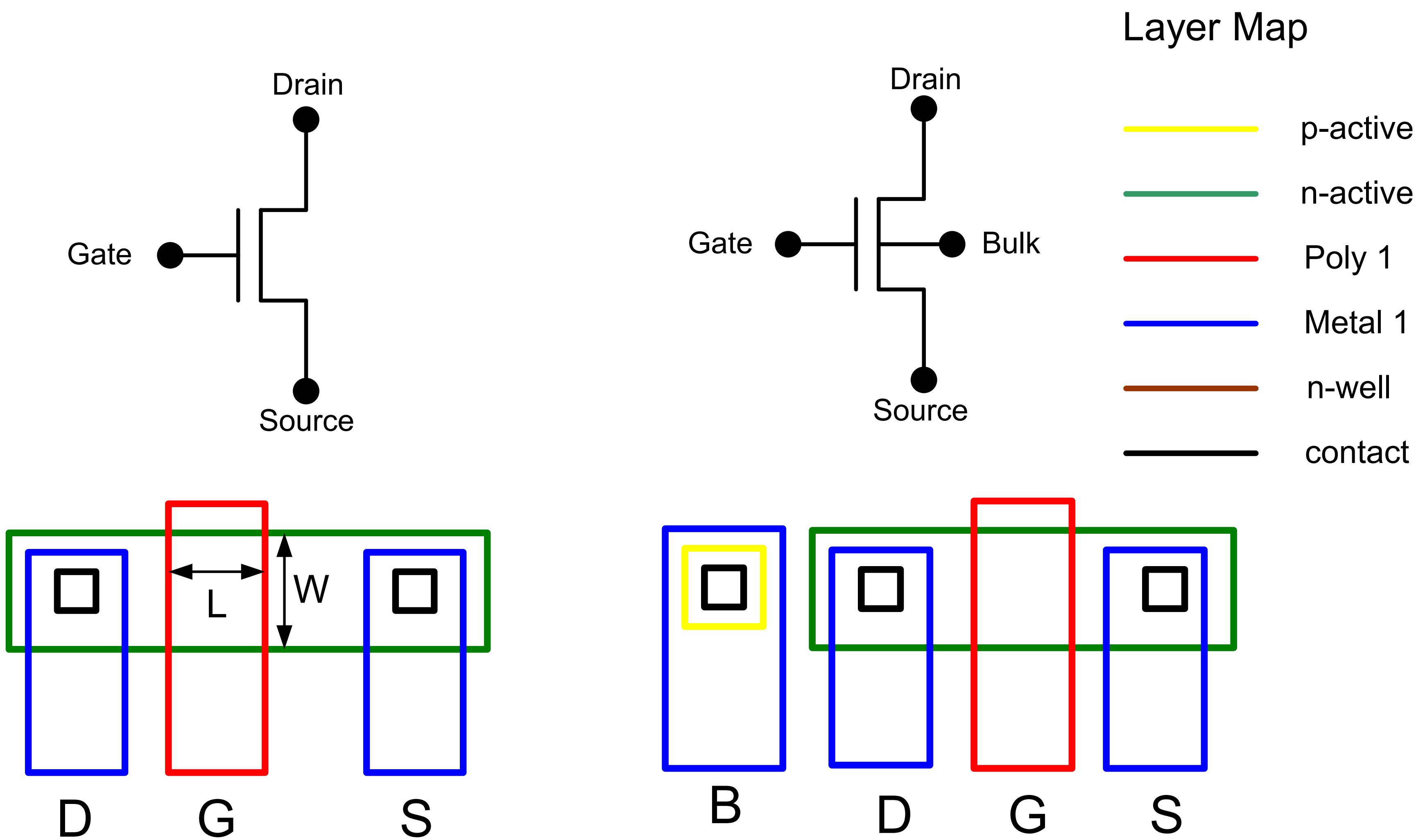


n-channel MOSFET



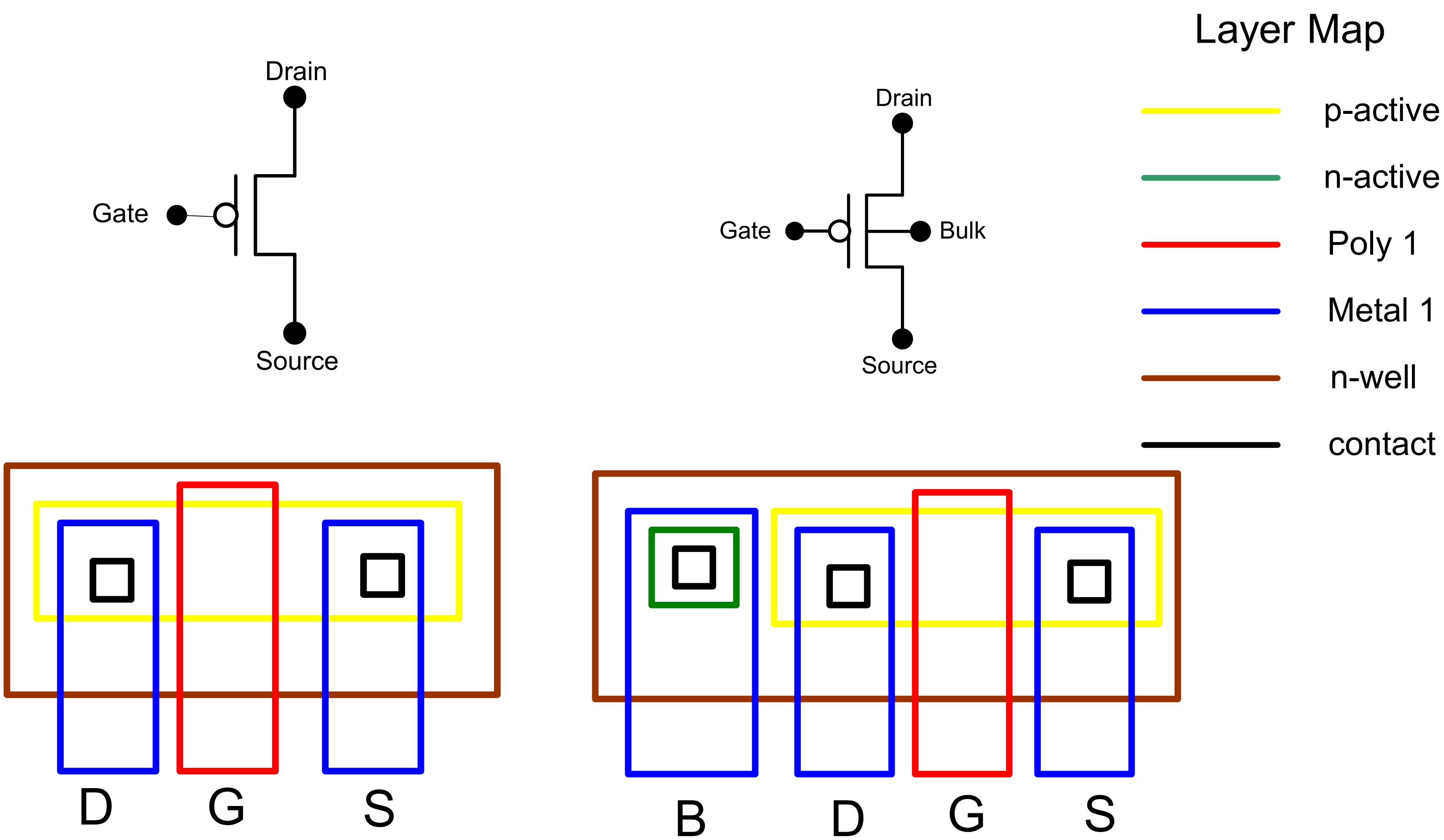
p-channel MOSFET

Design Rules and Layout – consider transistors



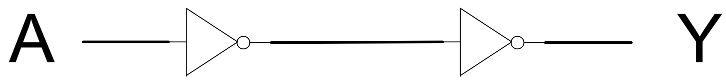
- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors

Design Rules and Layout – consider transistors

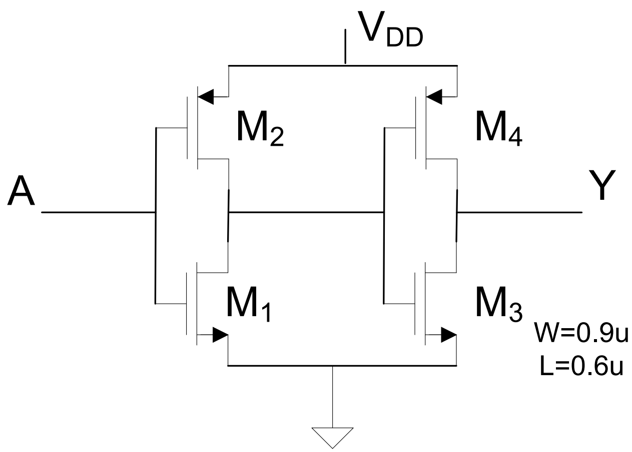


- Bulk connection needed
- Single bulk connection can often be used for several (many) transistors if they share the same well

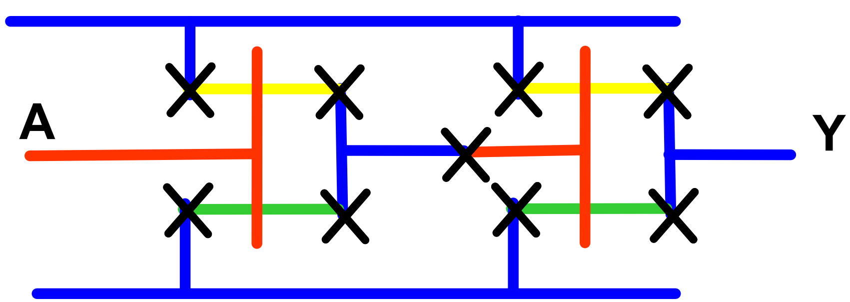
Design Rules and Layout (example)



Logic Circuit

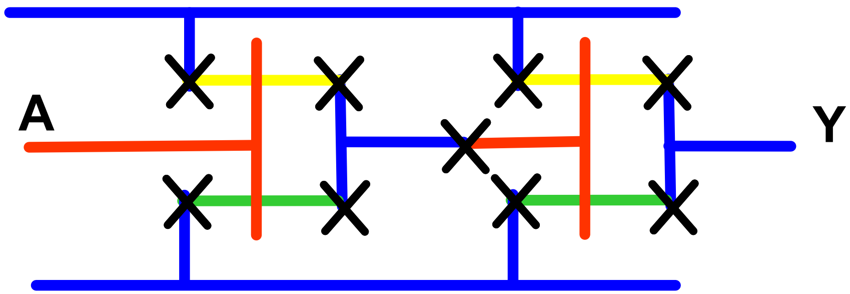


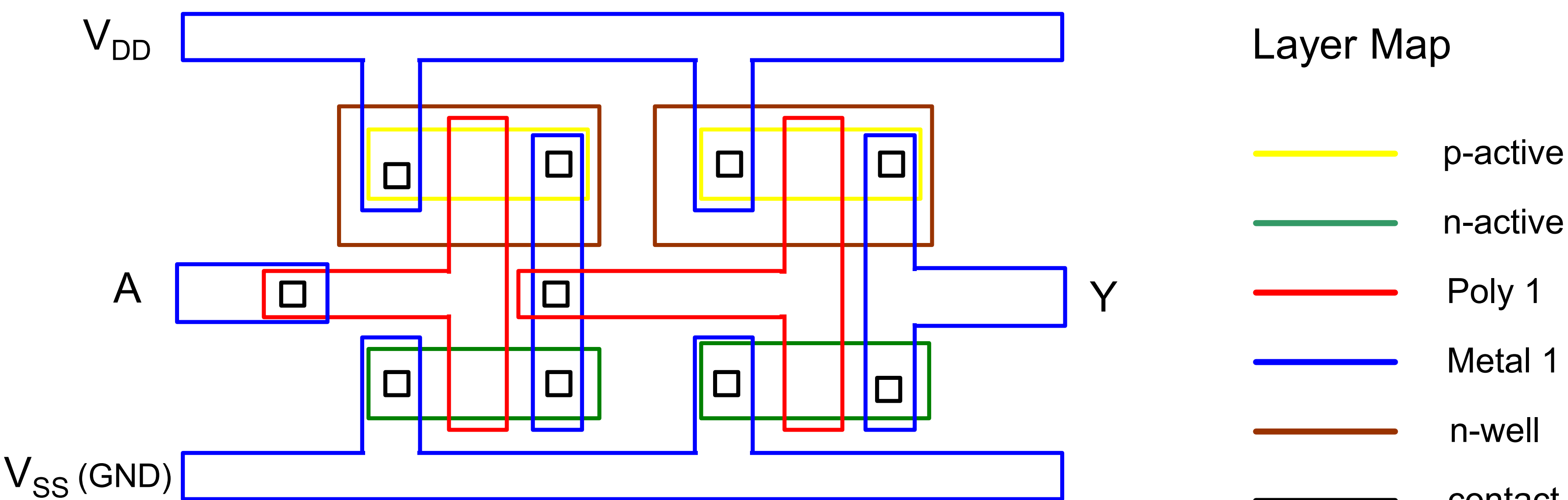
Circuit Schematic (Including Device Sizing)



Stick Diagram

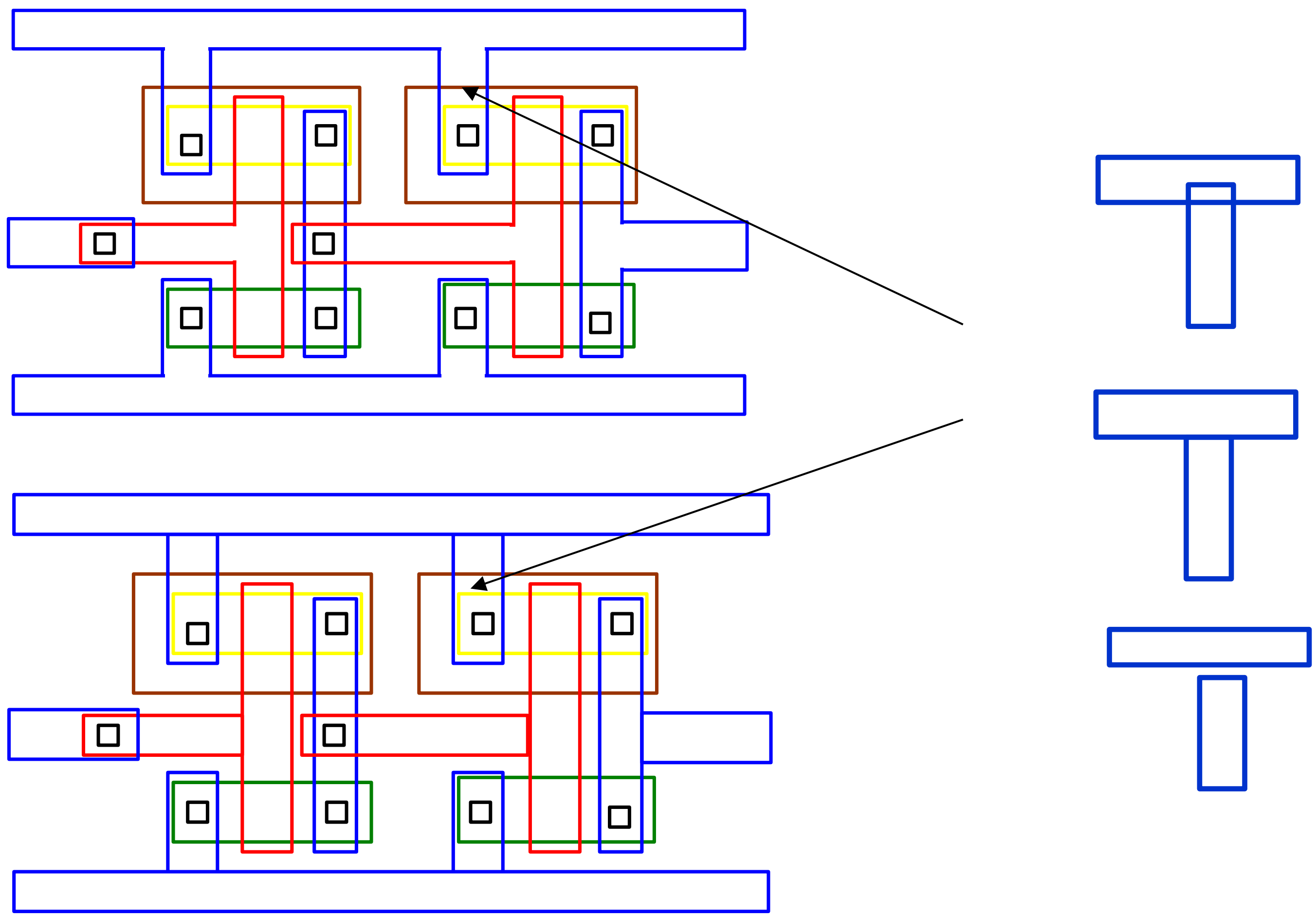
Design Rules (example)





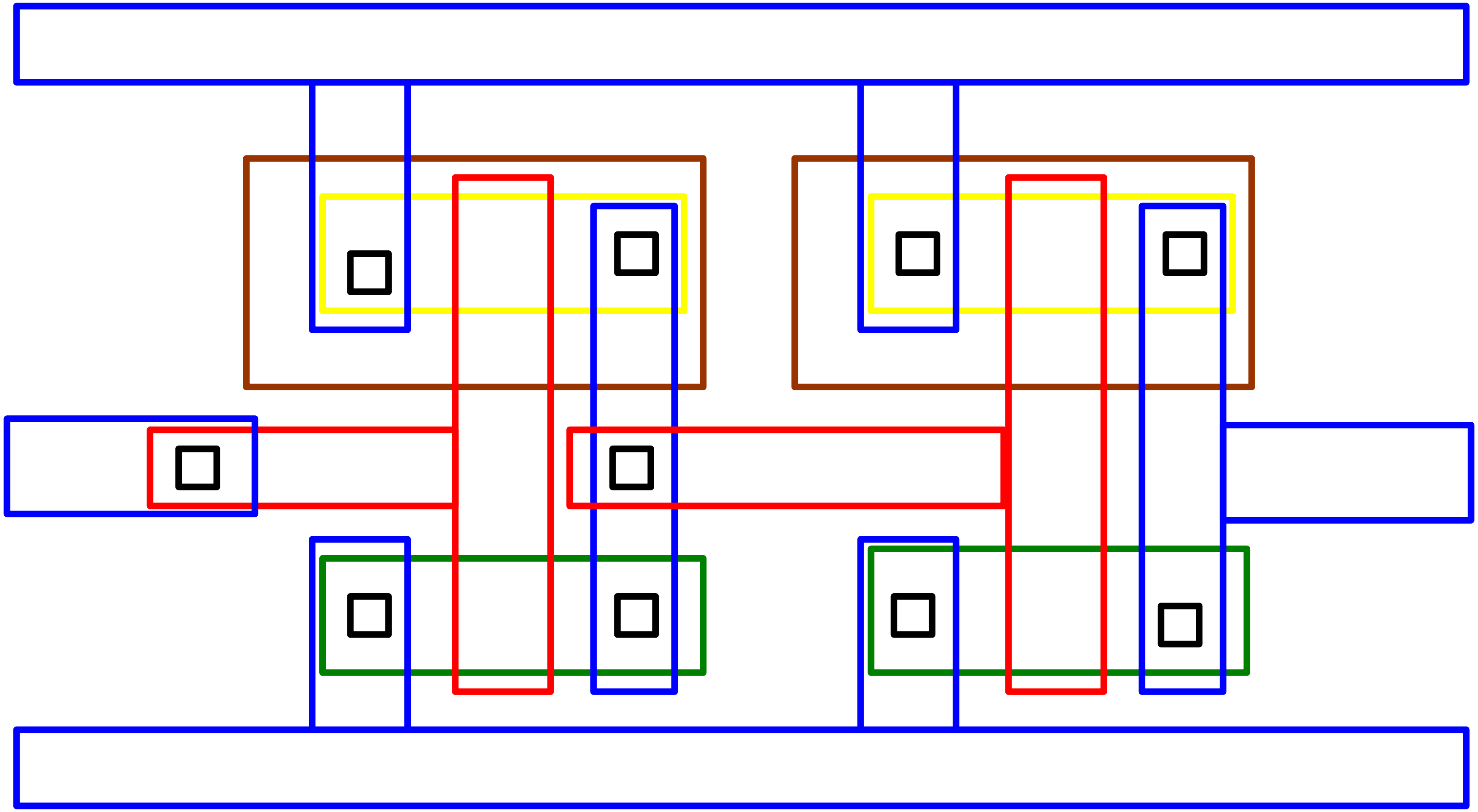
Layout

Design Rules (example)



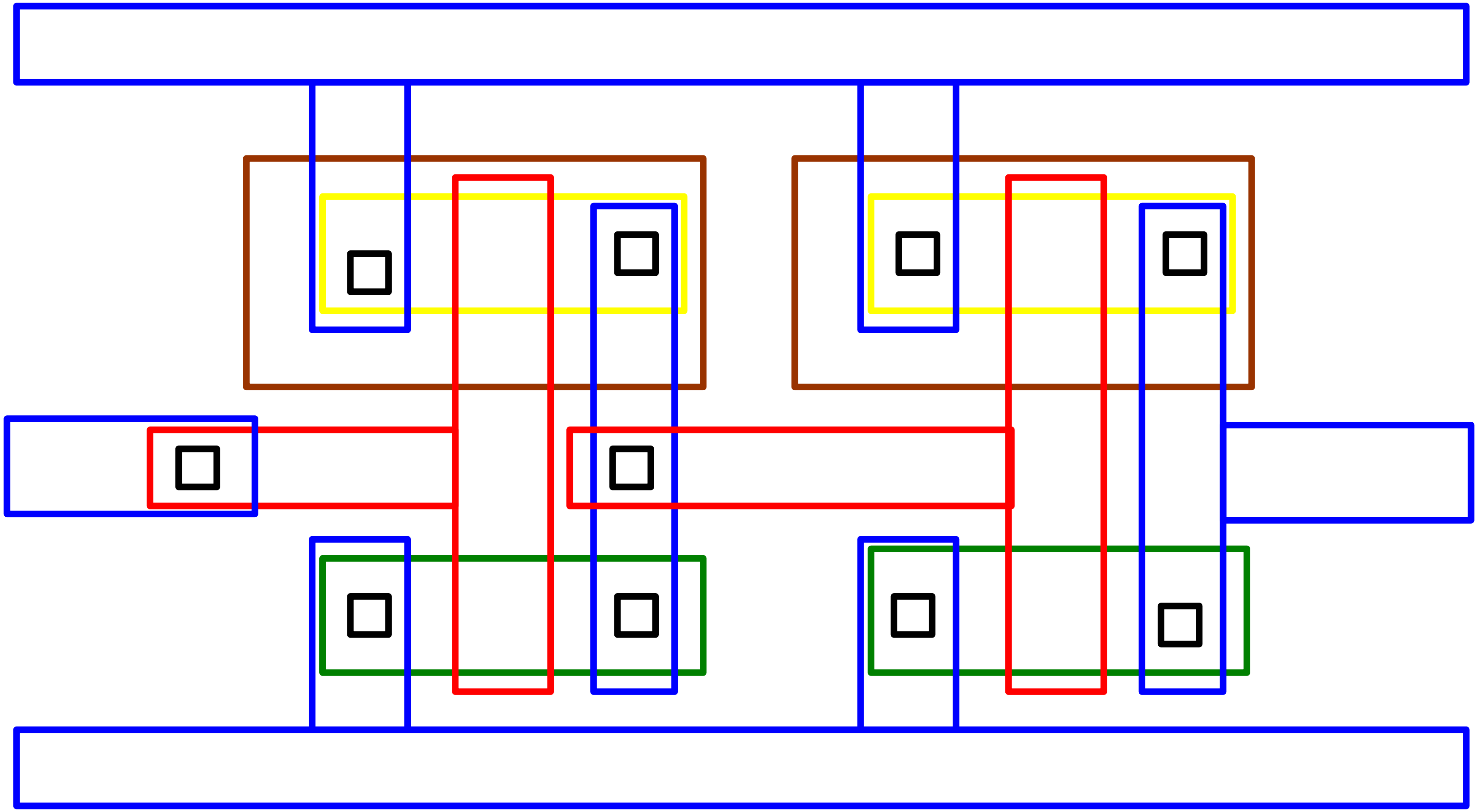
- Polygons in Geometric Description File (GDF) merged (when driving the pattern generator that makes the masks)
- Separate rectangles generally more convenient to represent
- Good practice to overlap rectangles to avoid break (though such an error would likely be caught with DRC)

Design Rules (example)



- Design rules must be satisfied throughout the design
- DRC runs incrementally during layout in most existing tools to flag most problems
- DRC can catch layout design rule errors but not circuit connection errors

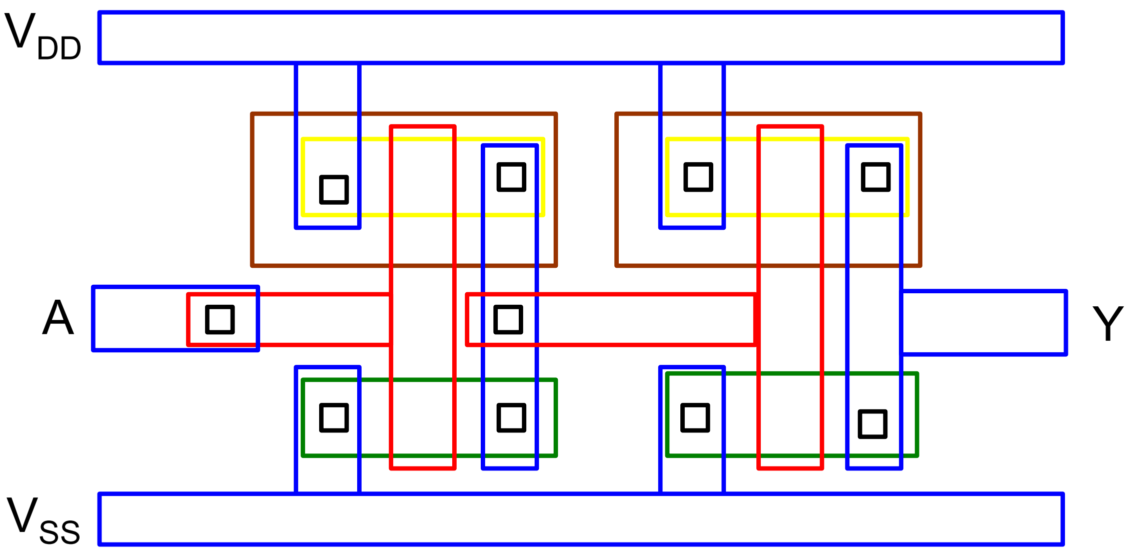
Design Rules (example)

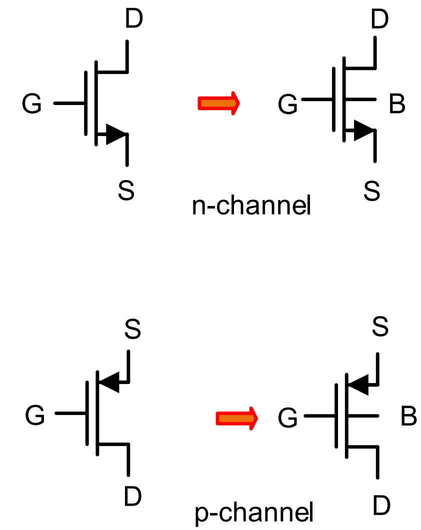


What is wrong with this layout ?

Bulk connections missing!

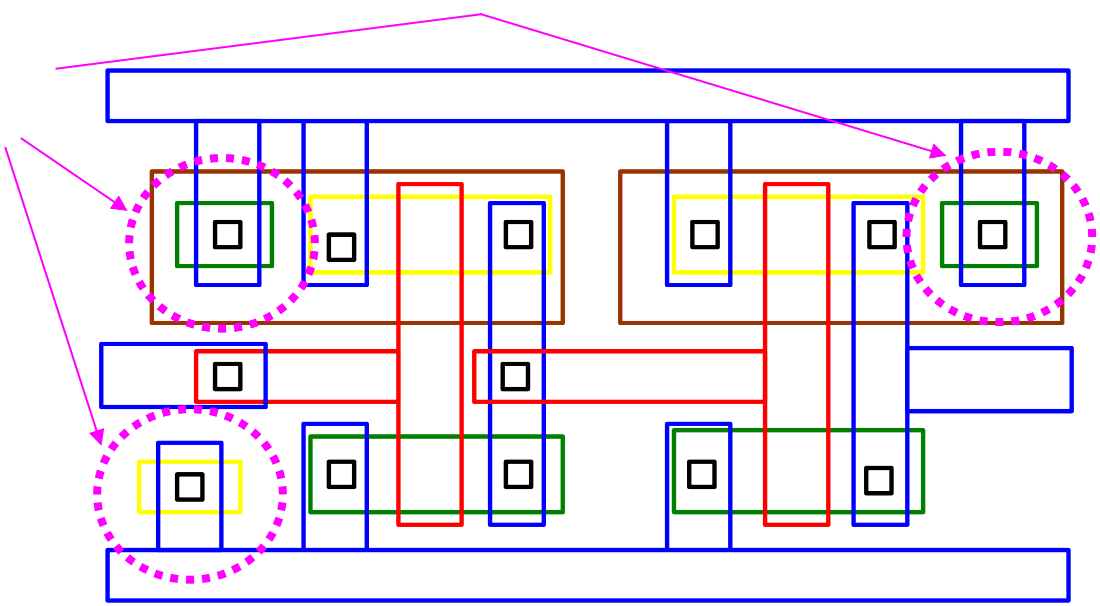
Design Rules (example)



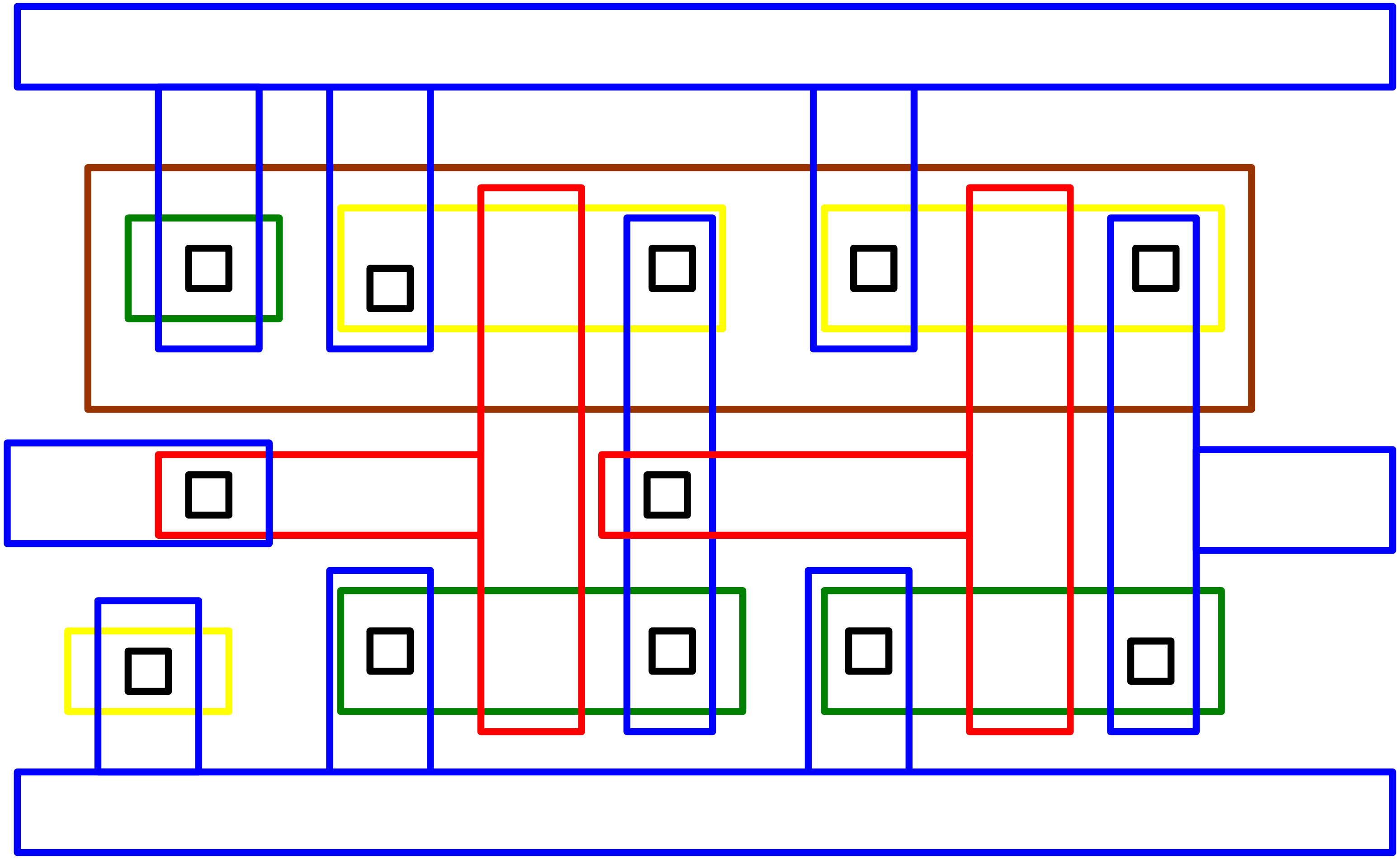


Actually 4-terminal device

- Note diffusions needed for bulk connections
- Note n-well connections increase area a significant amount
- Note n-wells are both connected to V_{DD} in this circuit

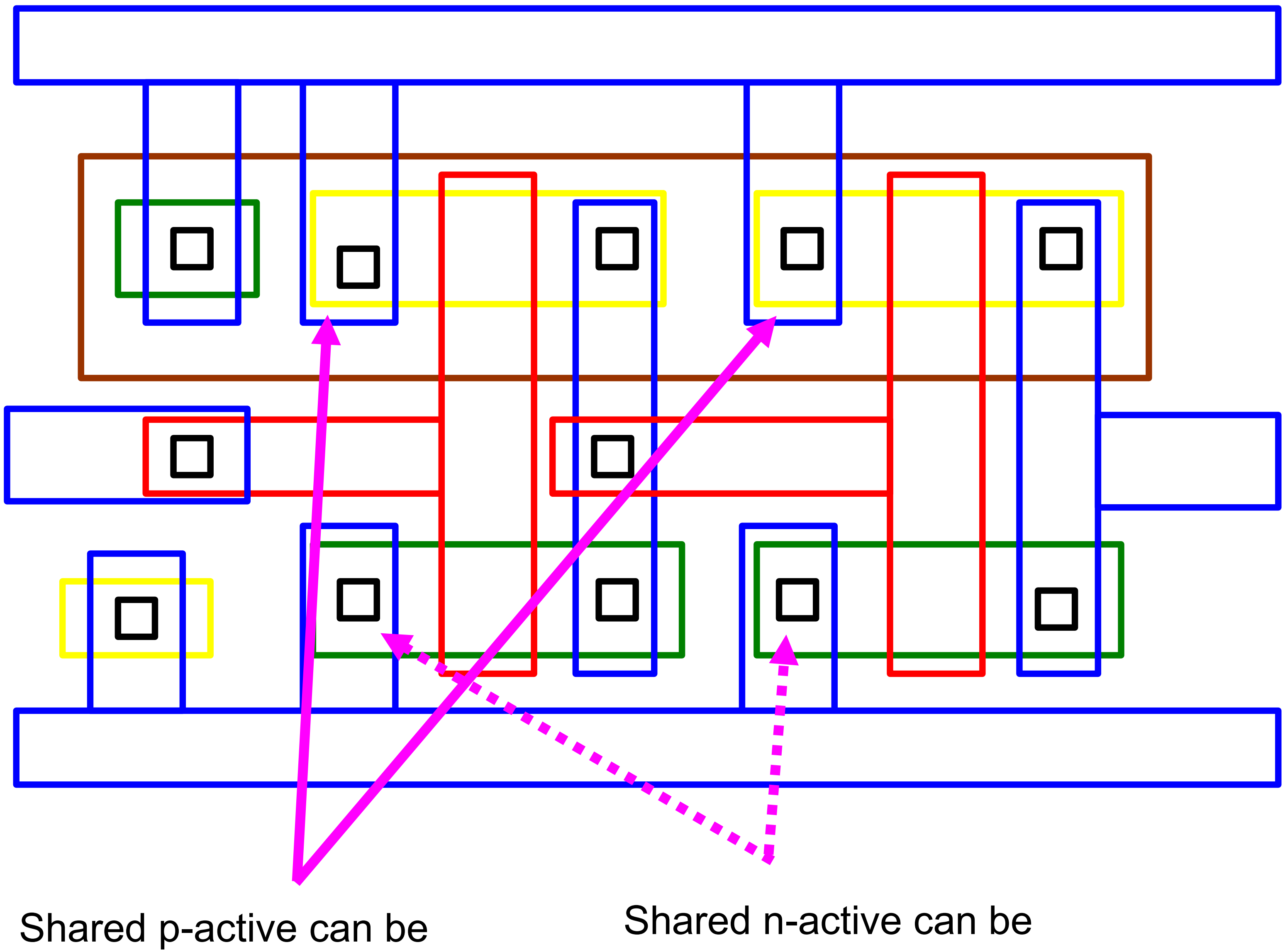


Design Rules (example)



Layout with shared n-well reduces area

Design Rules (example)



Design Rules

- Design rules can be given in absolute dimensions for every rule

- Design rules can be parameterized and given relative to a parameter
  - Makes movement from one process to another more convenient
  - Easier for designer to remember
  - Some penalty in area efficiency
  - Often termed λ-based design rules
  - Typically λ is ½ the minimum feature size in a process

Technology code with link to layer map	Layers
SCNE	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

Typical Technology →

SCMOS Layout Rules - Well

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9 [1]	18 [2]	18
1.3	Minimum spacing between wells at same potential	6 [3]	6 [4]	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0

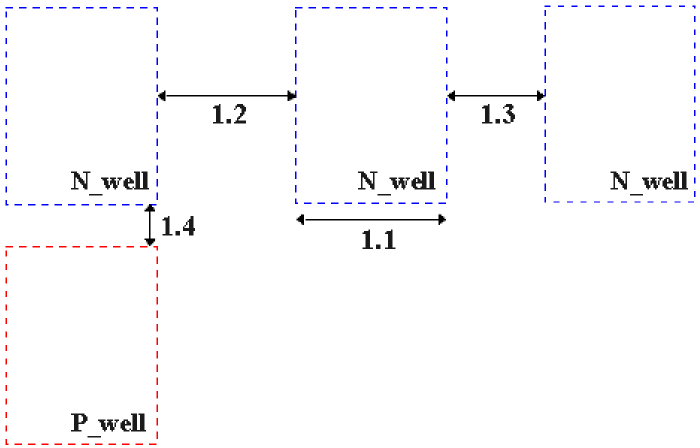
Exceptions for AMIS C30 0.35 micron process:

[1] Use lambda=16 for rule 1.2 only when using SCN4M or SCN4ME

[2] Use lambda=21 for rule 1.2 only when using SCN4M_SUBM or SCN4ME_SUBM

[3] Use lambda=8 for rule 1.3 only when using SCN4M or SCN4ME

[4] Use lambda=11 for rule 1.3 only when using SCN4M_SUBM or SCN4ME_SUBM



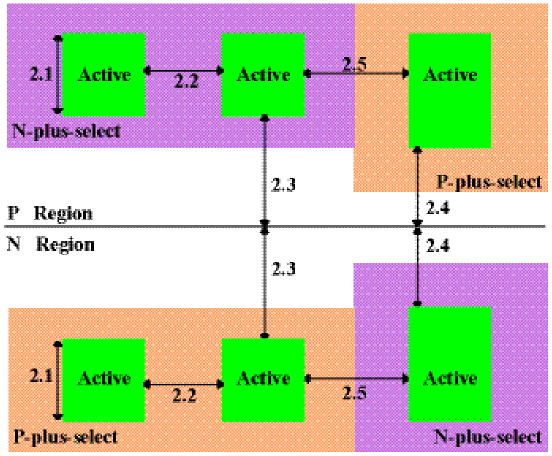
Technology code with link to layer map	Layers
SCNE	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

SCMOS Layout Rules - Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4

* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for AMIS designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

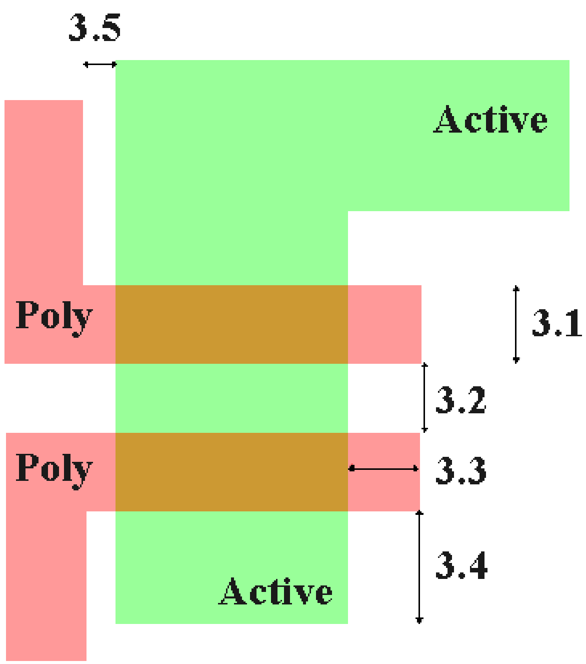
Process	Design Technology	Design Lambda (micrometers)	Minimum Width (lambda)
AMI_ABN	SCNA, SCNE	0.80	5
AMI_C5F/N	SCN3M, SCN3ME	0.35	9
AMI_C5F/N	SCN3M_SUBM, SCN3ME_SUBM	0.30	10



Technology code with link to layer map	Layers
SCNE	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

SCMOS Layout Rules - Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



Technology code with link to layer map	Layers
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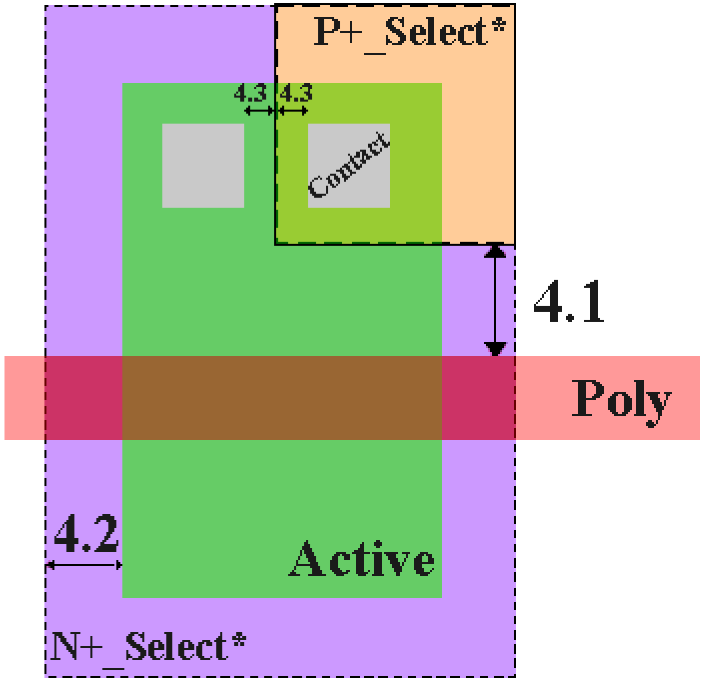
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

Select – Active(moat) Concepts

- Note that there is no n-active or p-active masks
- n-channel devices which need n-active are created by overlaying active with n-select
- p-channel devices which need p-active are created by overlaying active with p-select
- n-select and p-select masks are somewhat larger than the desired n-active and p-active regions

SCMOS Layout Rules - Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	2	4



*The same rules apply with N+_Select and P+_Select reversed.

Pictorial Description of Typical Design Rules

Class WEB site:

Reference material

- Complete CMOS process flow (PowerPoint file)
- Pictorial Design Rules (Most basic rules in one PDF files)
- NXP Thyristor Application Note
- ON Thyristor Application Note
- National Thysistor Application Note
- Selected Data Sheets

Table 5: Technology-code Map

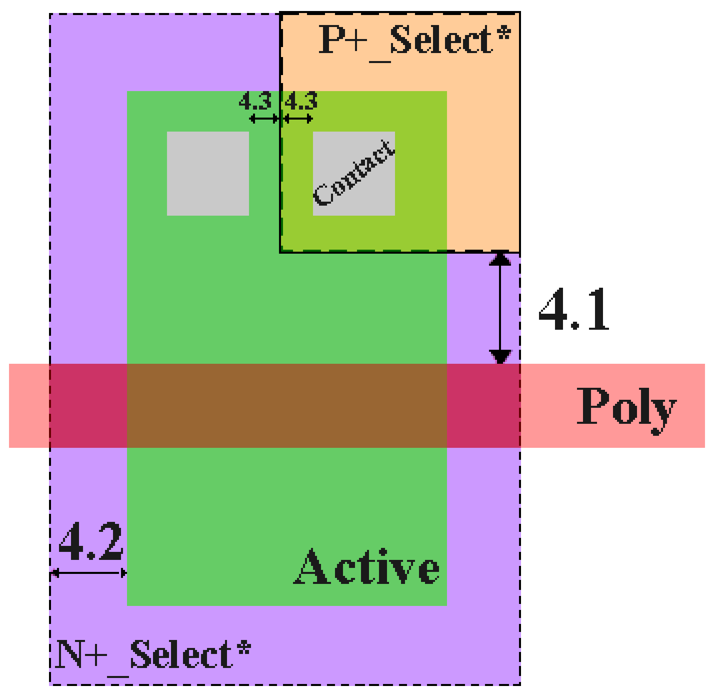
Technology code with link to layer map	Layers
SCNE	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Metal1, Via, Metal2, Glass
SCNA	N_well, Active, N_select, P_select, Poly, Poly2, Contact, Pbase, Metal1, Via, Metal2, Glass
SCNPC	N_well, Active, N_select, P_select, Poly_cap, Poly, Contact, Metal1, Via, Metal2, Glass
SCN3M	N_well, Active, N_select, P_select, Poly, Silicide block (Agilent/HP only), Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass
SCN3ME	N_well, Active, N_select, P_select, Poly, Poly2, Hi_Res_Implant, Contact, Metal1, Via, Metal2, Via2, Metal3, Glass

Select – Active(moat) Concepts

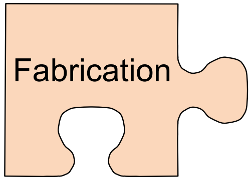
- Note that there is no n-active or p-active masks
- n-channel devices which need n-active are created by overlaying active with n-select
- p-channel devices which need p-active are created by overlaying active with p-select
- n-select and p-select masks are somewhat larger than the desired n-active and p-active regions

SCMOS Layout Rules - Select

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	2	4



*The same rules apply with N+_Select and P+_Select reversed.



Technology Files

- Design Rules

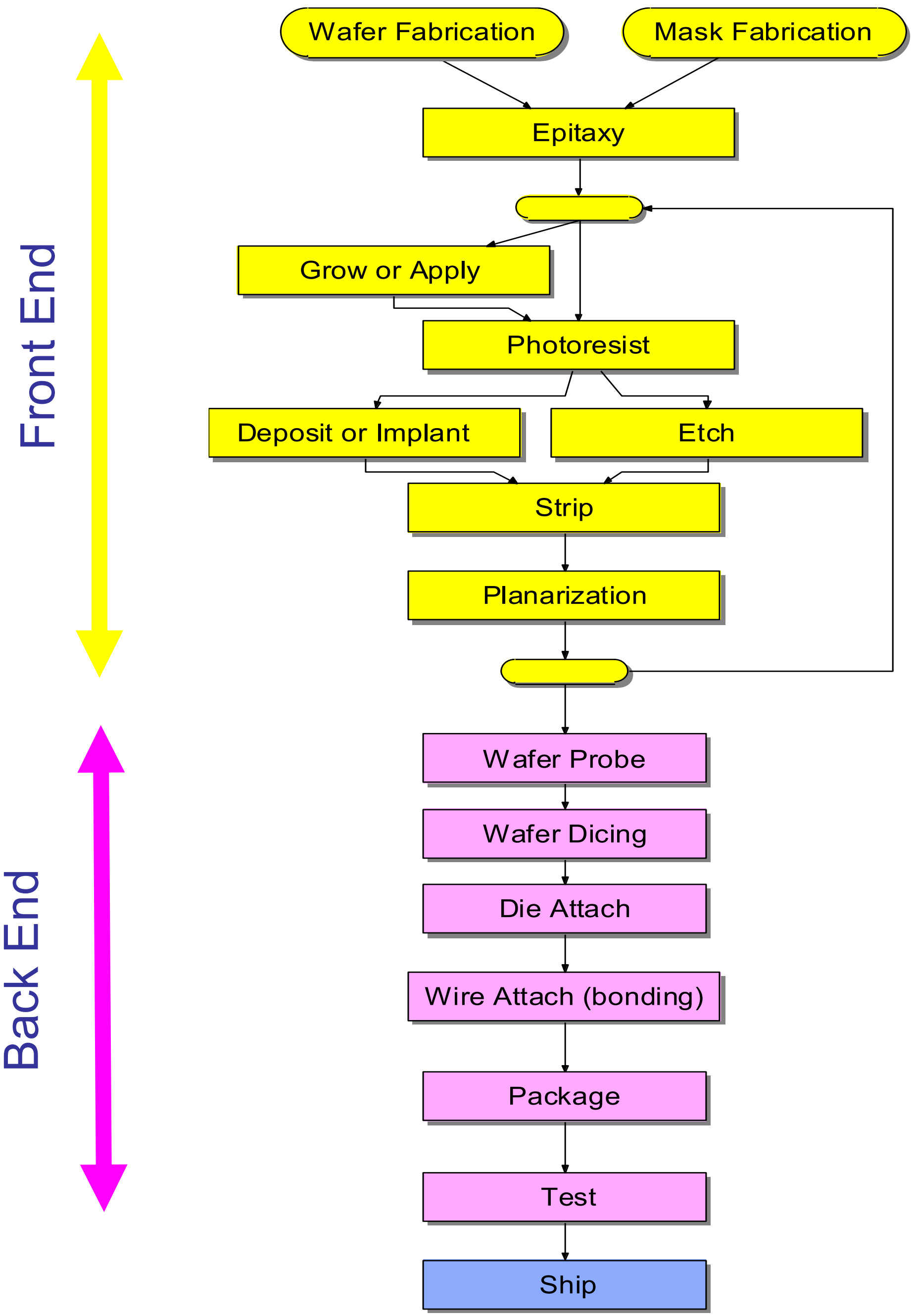
Process Flow (Fabrication Technology)

- Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)

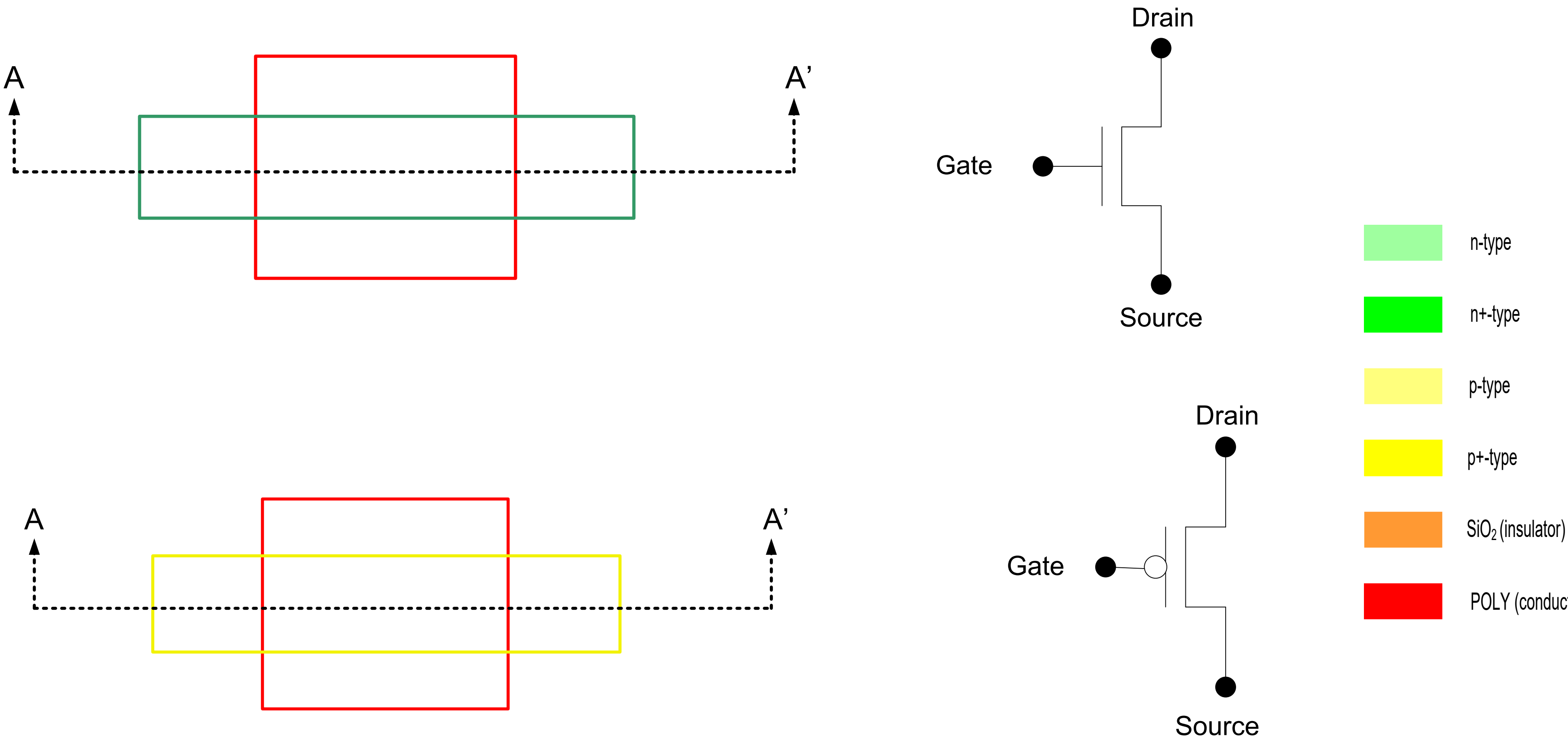
IC Fabrication Technology

See Chapter 3 and a little of Chapter 1 of WH

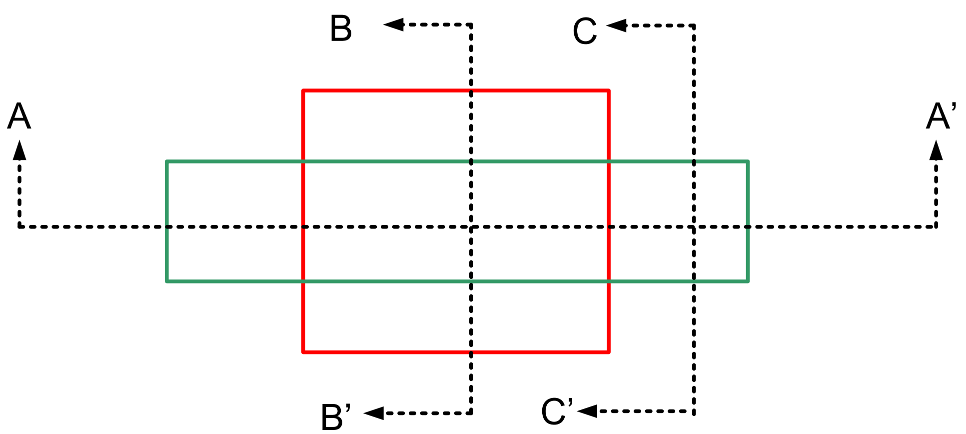
Generic Process Flow

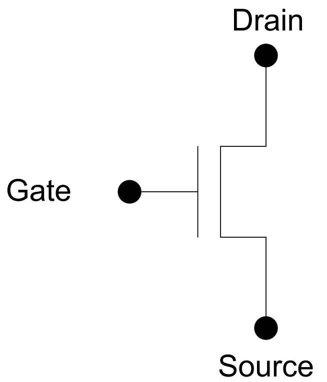


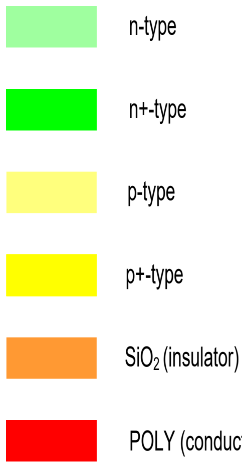
First a bit of background on transistor structure



First a bit of background on transistor structure



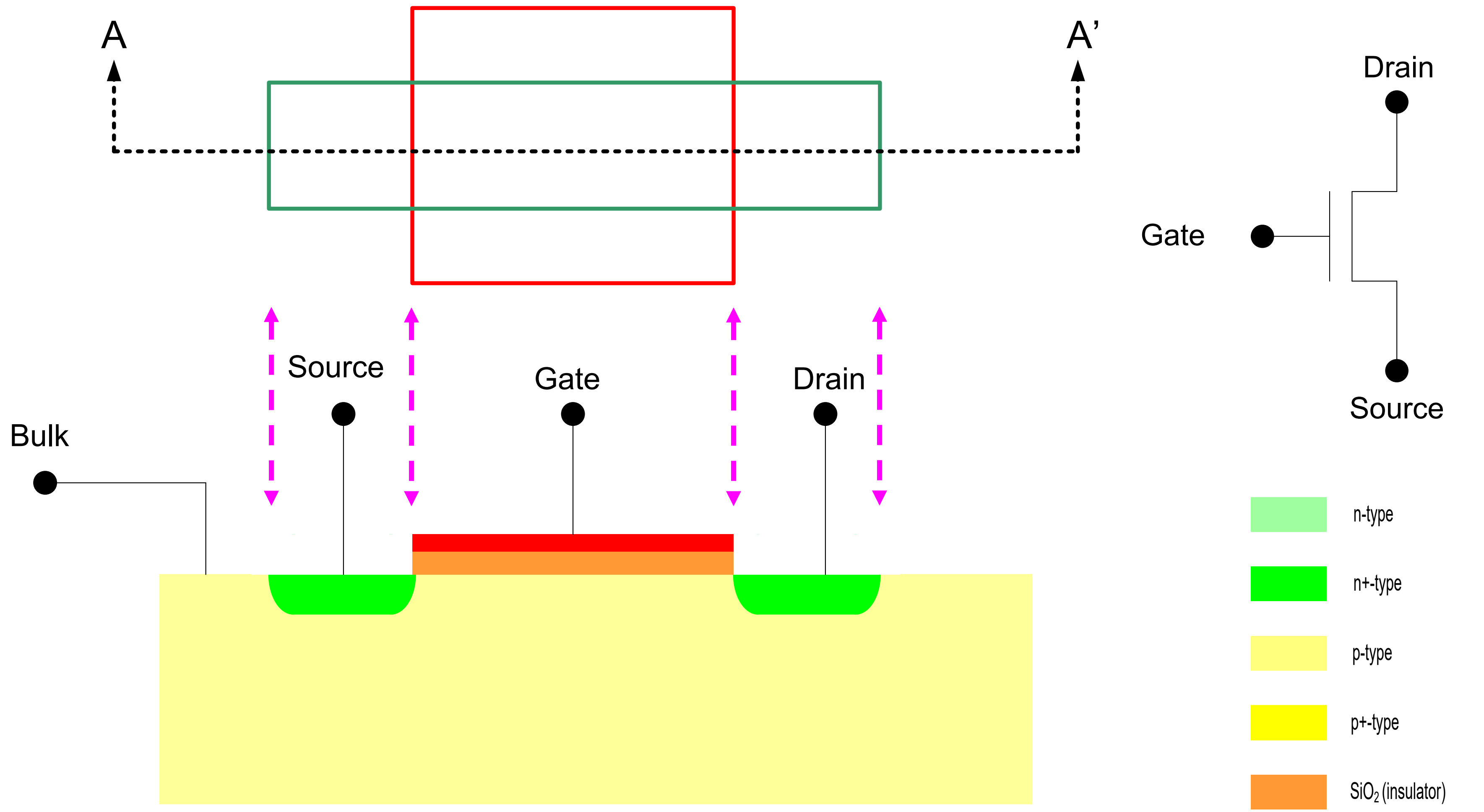




Looks Different on Other Cross-Sections !

Recall

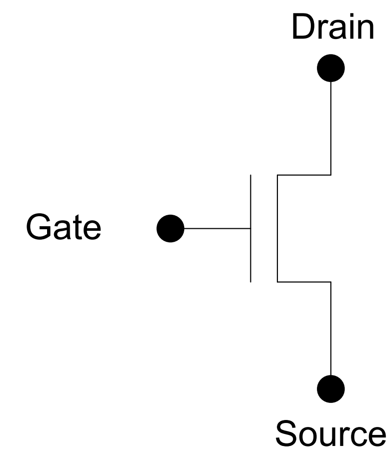
MOS Transistor

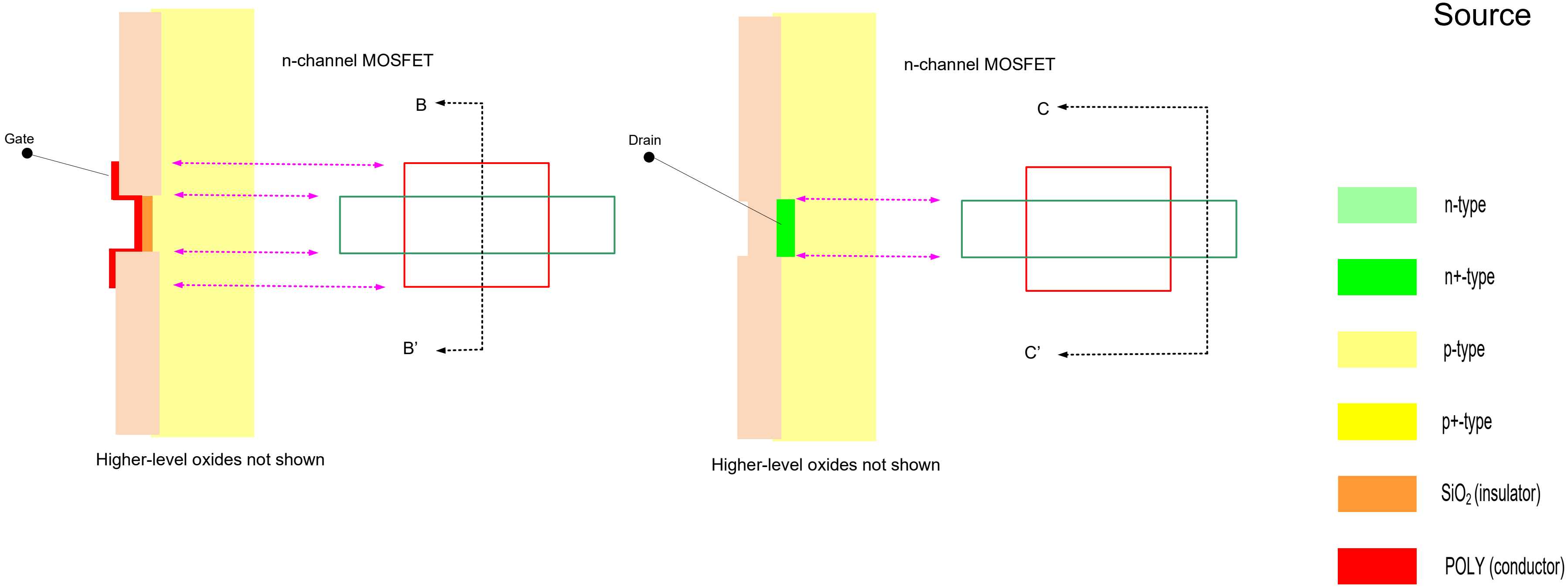


n-channel MOSFET

Higher level oxides not shown

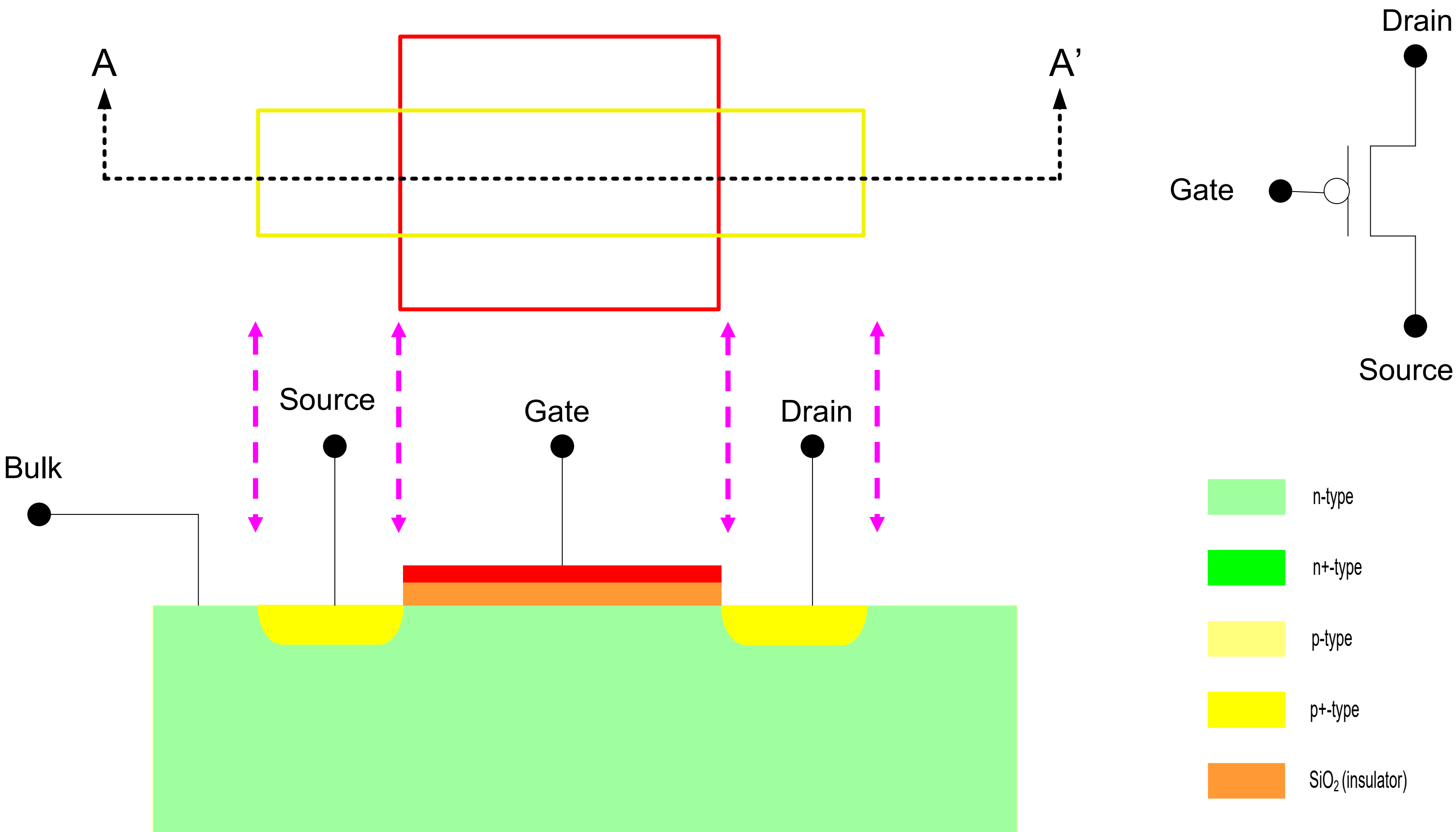
MOS Transistor





Review

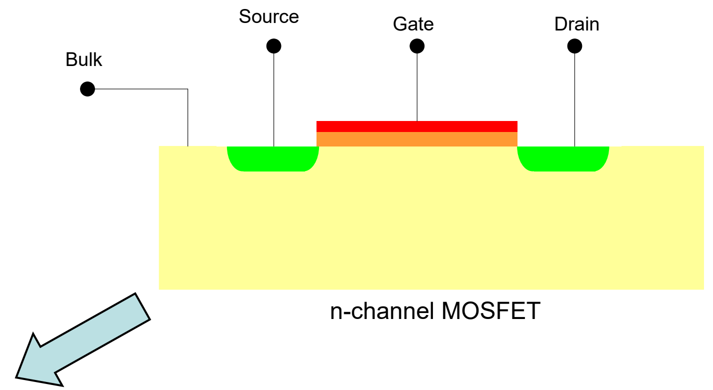
MOS Transistor

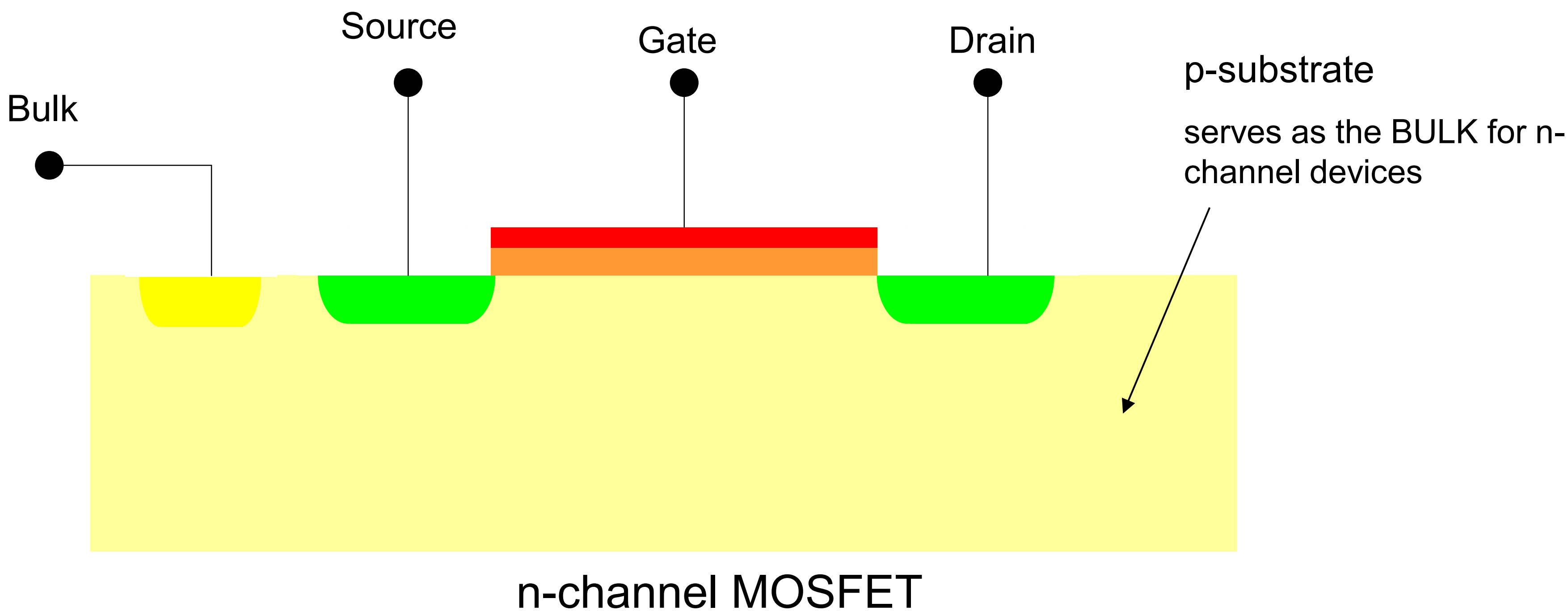


p-channel MOSFET

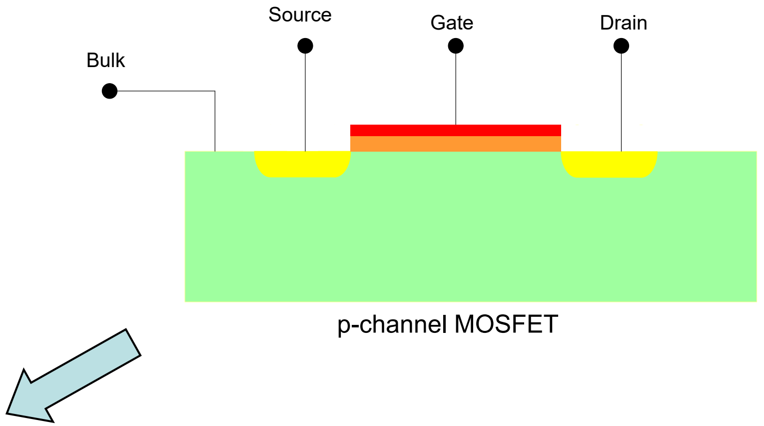
MOS Transistor

n-channel MOS transistor in
Bulk CMOS n-well process
with bulk contact

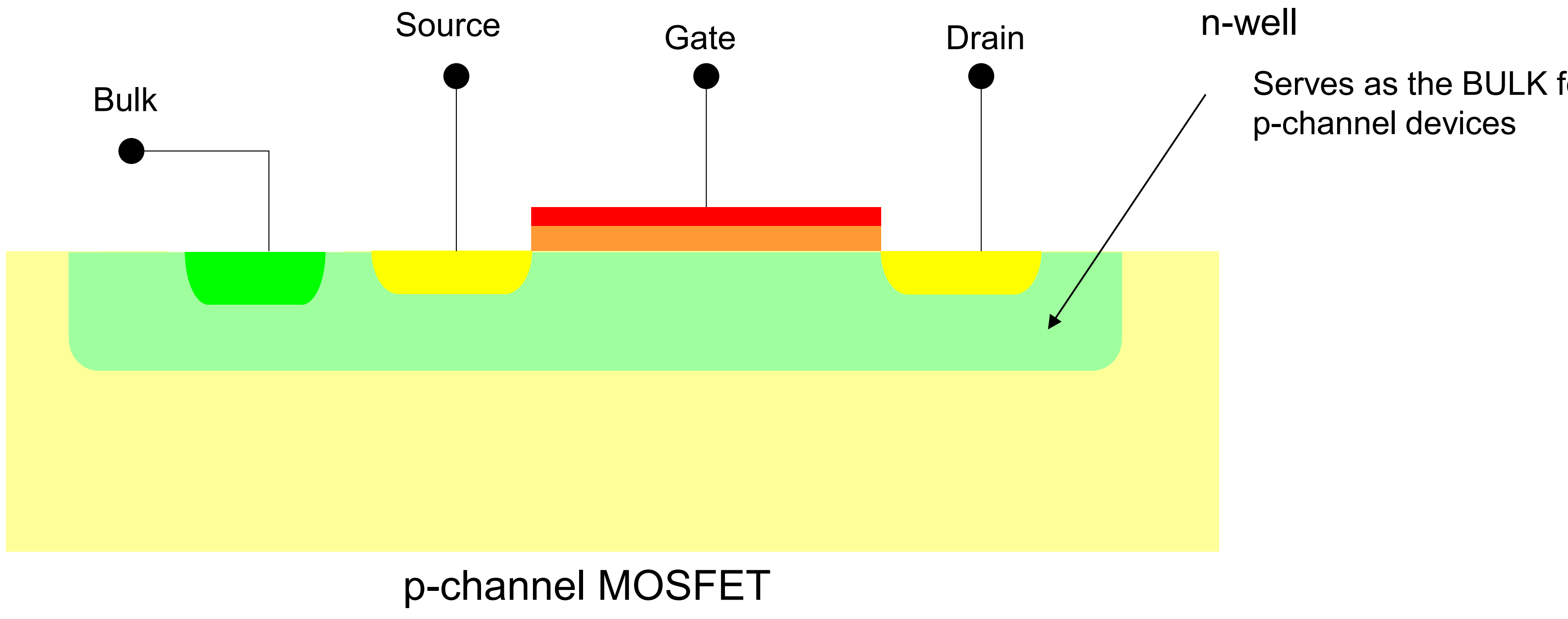




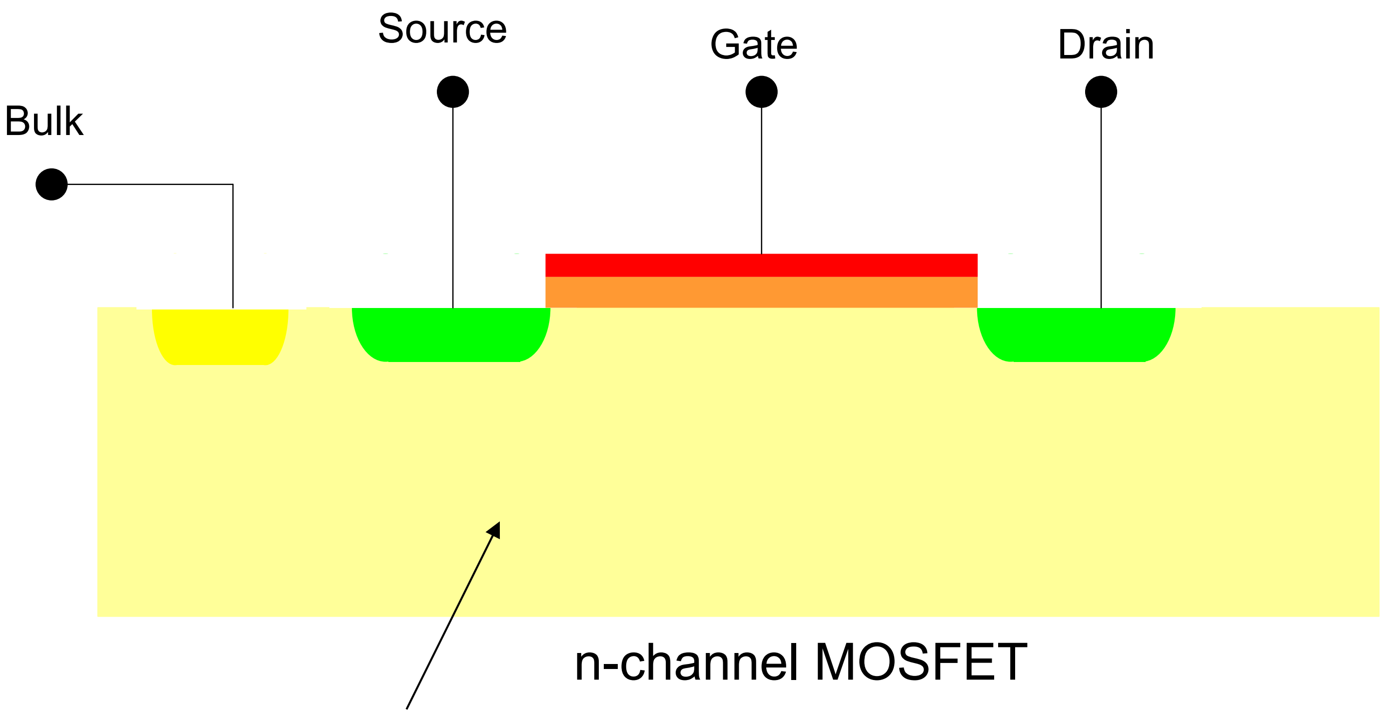
MOS Transistor



p-channel MOS transistor in Bulk CMOS n-well process with bulk contact and well (tub)

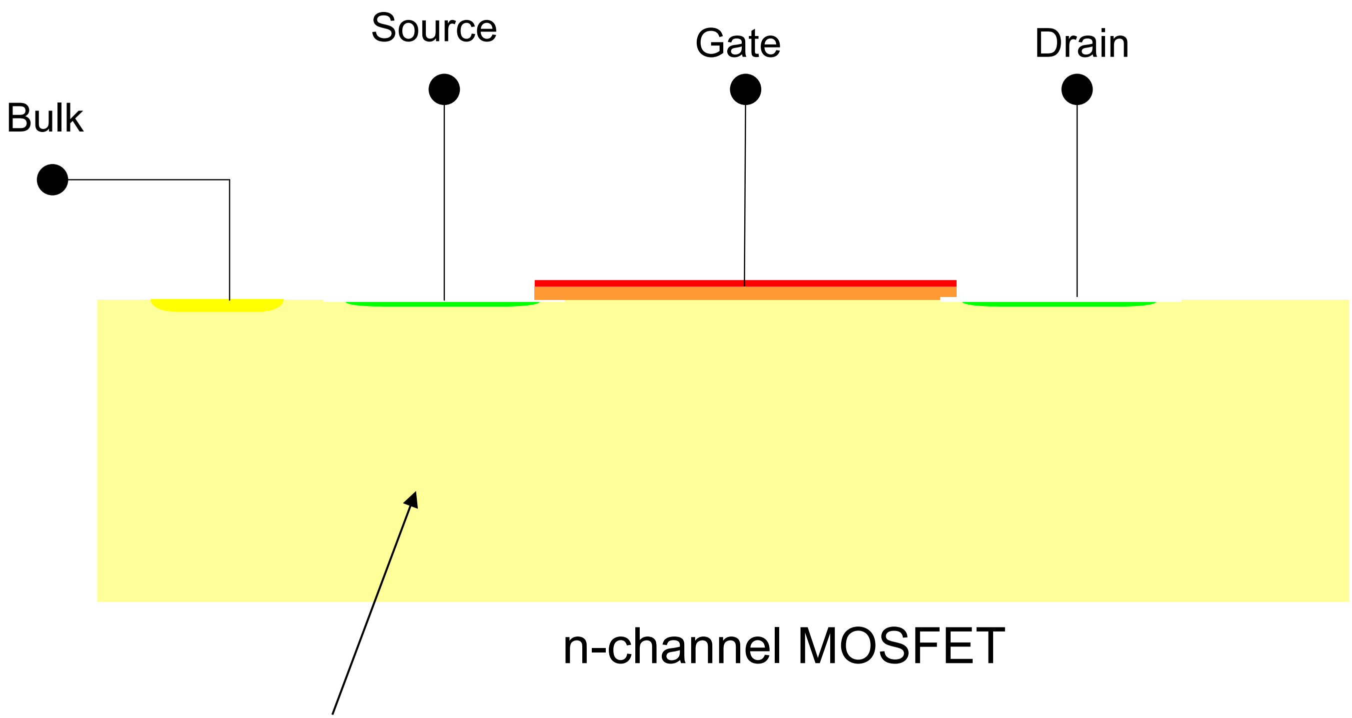


MOS Transistor



- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the Bulk

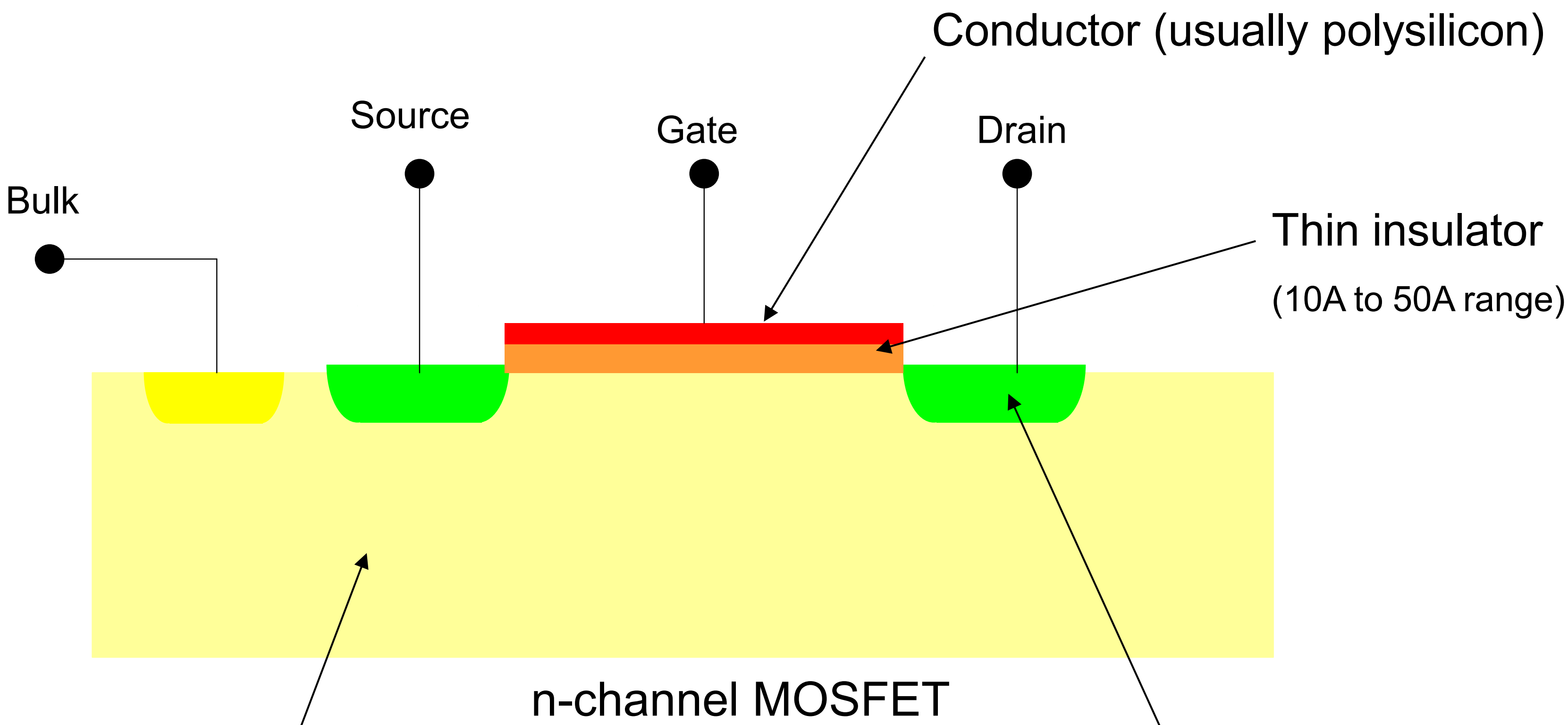
MOS Transistor



n-channel MOSFET

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

MOS Transistor

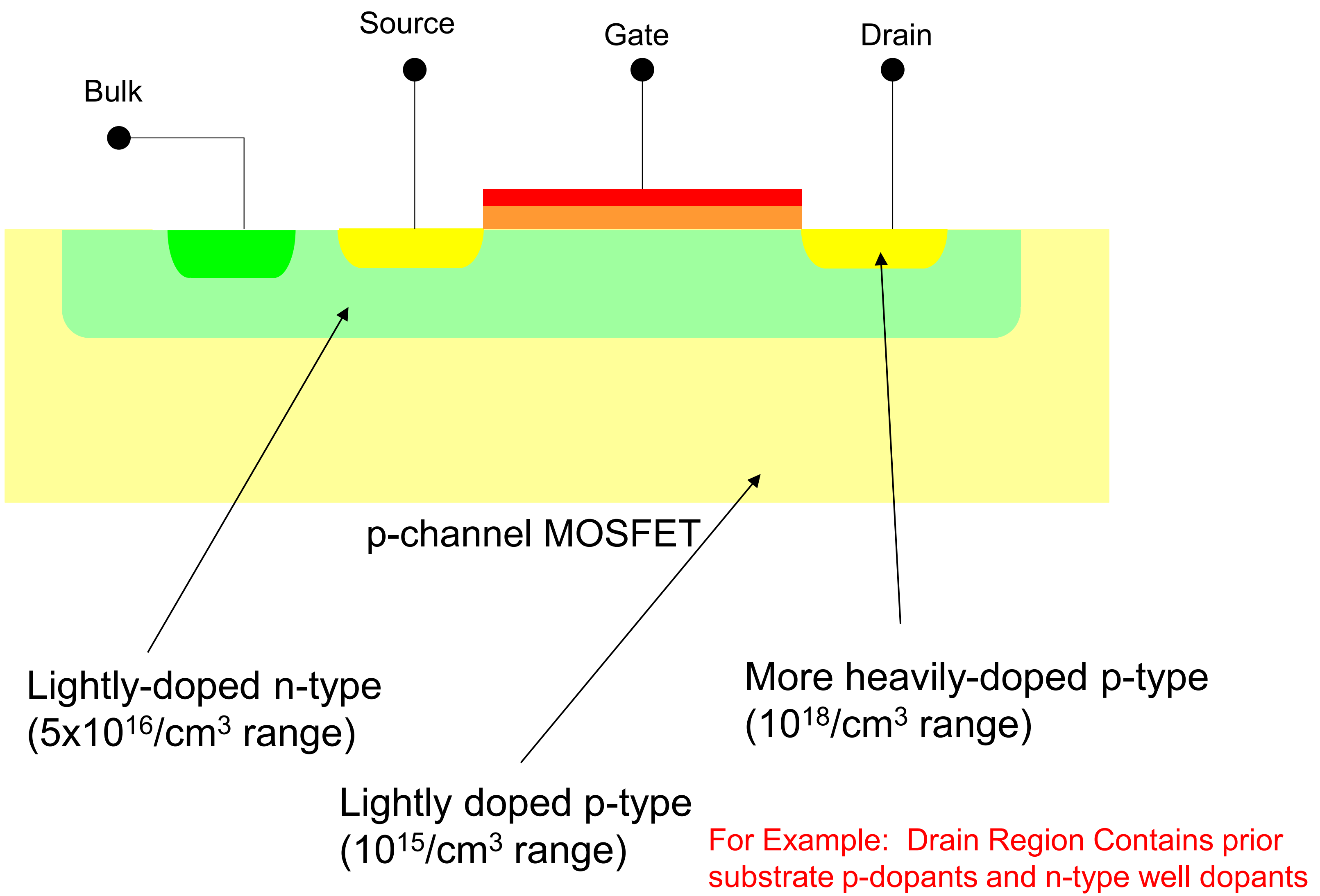


More heavily doped ($10^{17}/cm^3$ range)

- Single-crystalline silicon
  - Serves as physical support member
  - Lightly doped (p-doping in the $10^{15}/cm^3$ range, silicon atoms in the $2.2x10^{22}/cm^3$ range)
  - Vertical dimensions are not linearly depicted
  - Often termed the BULK

Dominant Doping Depicted – Generally Contain Prior Lower Density Dopants of Opposite Type

MOS Transistor



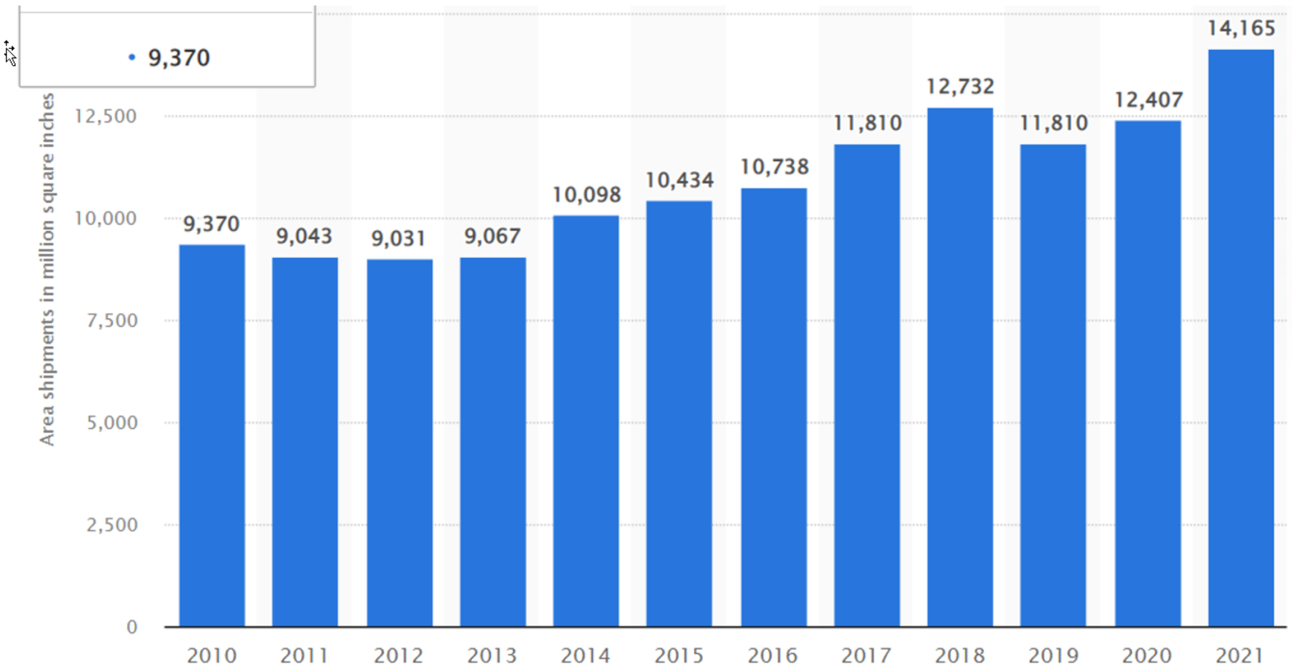
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Ion Imlantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Planarization
- Contacts, Interconnect and Metalization

Crystal Preparation

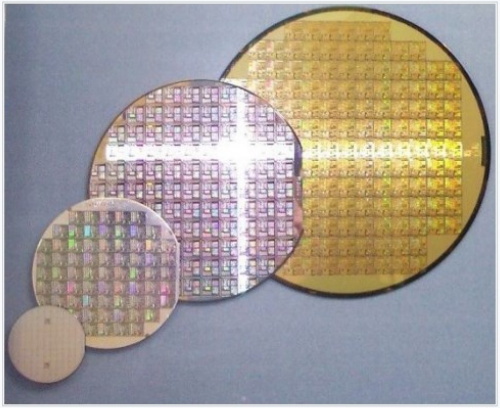
- Large crystal is grown (pulled)
  - 12 inches (300mm) in diameter and 1 to 2 m long
  - Sliced to 250µm to 500µm thick
    - Prefer to be much thinner but thickness needed for mechanical integrity
  - 4 to 8 cm/hr pull rate
  - T=1430 ^{o}C
- Crystal is sliced to form wafers
- Cost for 12” wafer around $200
- 5 companies provide 90% of worlds wafers
- Somewhere around 400,000 12in wafers/month

Silicon wafer area is a better metric



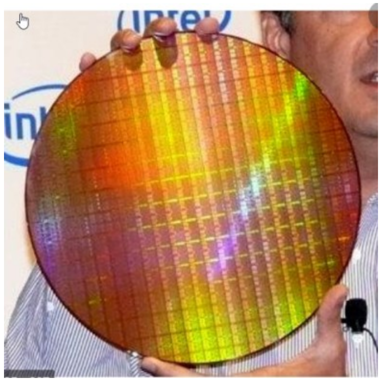
Crystal Preparation

Wafer size	Typical Thickness	Year Prodn [15]	Weight per wafer	100 mm2 (10 mm) Die per wafer [hide]
1-inch (25 mm)		1960		
2-inch (51 mm)	275 μm	1969		
3-inch (76 mm)	375 μm	1972		
4-inch (100 mm)	525 μm	1976	10 grams [19]	56
4.9 inch (125 mm)	625 μm	1981		
150 mm (5.9 inch, usually referred to as "6 inch")	675 μm	1983		
200 mm (7.9 inch, usually referred to as "8 inch")	725 μm.	1992	53 grams [19]	269
300 mm (11.8 inch, usually referred to as "12 inch")	775 μm	2002	125 grams[19]	640
450 mm (17.7 inch) (proposed).[20]	925 μm	future	342 grams [19]	1490
675-millimetre (26.6 in) (Theoretical).[21]	Unknown.	future		

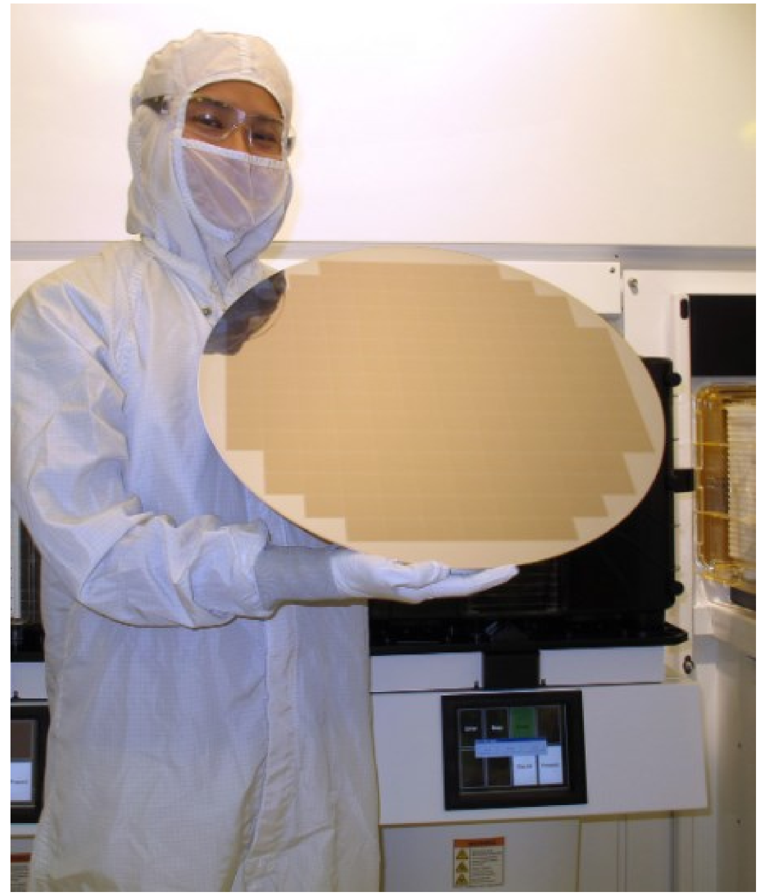


2-inch (51 mm), 4-inch (100 mm), 6-inch (150 mm), and 8-inch (200 mm) wafers

Crystal Preparation

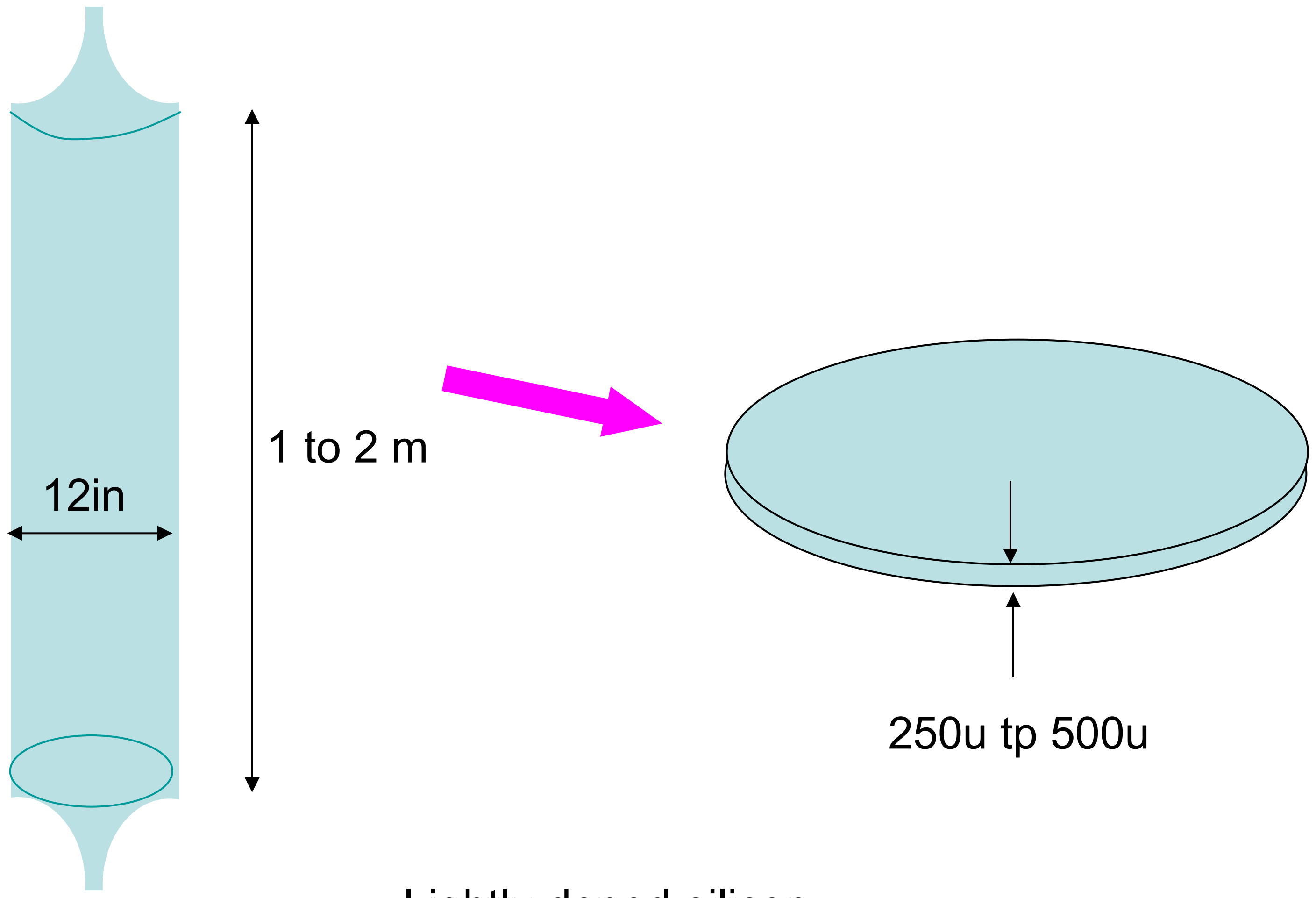


300mm wafer



450 mm wafer

Crystal Preparation



Some predicted newer FABs will be at 450mm (18in) by 2020 but appears to be uncertain whether it will ever happen

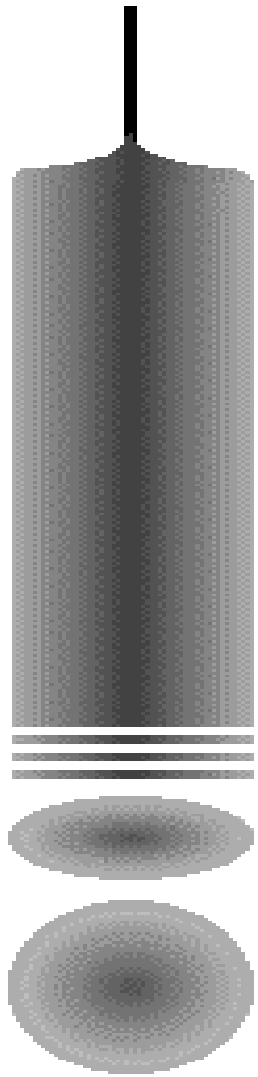
Lightly-doped silicon
Excellent crystalline structure

Crystal Preparation

Return on Investment Essential to Make Transition

200mm (8”) and 300mm (12”) are dominant in production today

Crystal Preparation

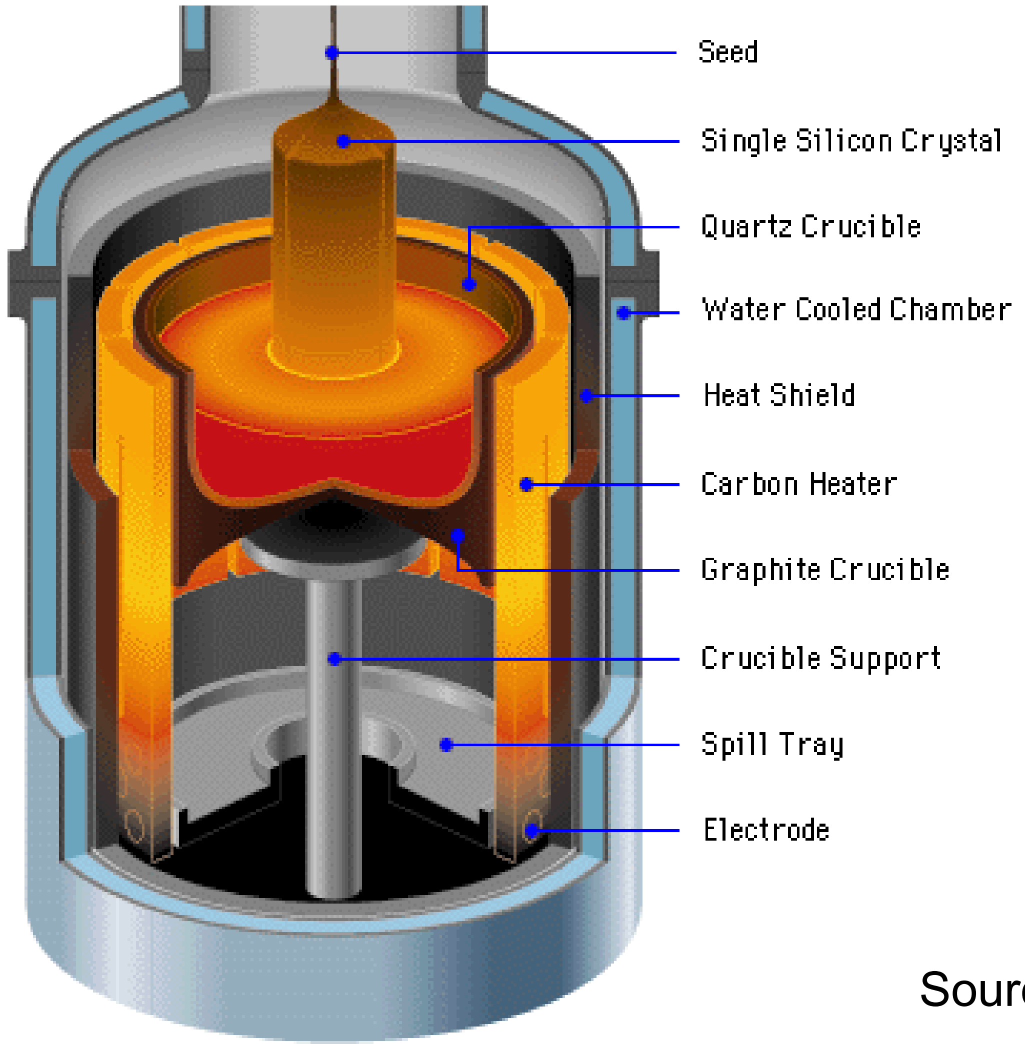


From www.infras.com

Crystal Preparation

Source: WEB

Crystal Preparation



Source: WEB

Crystal Preparation

Source: WEB

Crystal Preparation

A section of 300mm ingot is loaded into a wiresaw

Source: WEB

Crystal Preparation

Source: WEB

Stay Safe and Stay Healthy !

End of Lecture 8